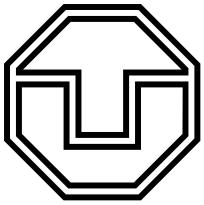

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Fabrication and characterization of a silicon nanowire based Schottky-barrier field effect transistor platform for functional electronics and biosensor applications

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to take the degree of
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Herstellung und Charakterisierung einer Silizium-Nanodraht basierten Schottky-Barrieren-Feld-Effekt-Transistor-Plattform für funktionelle Elektronik und Biosensoranwendungen

Dissertation
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ABSTRACT

This work focuses on the evaluation of the feasibility to employ silicon (Si) nanowire based parallel arrays of Schottky-barrier field effect transistors (SB-FETs) as transducers for potentiometric biosensors and their overall performance as building blocks for novel functional electronics. Nanowire parallel arrays of SB-FETs were produced and electrically characterized during this work. Nominally undoped Si nanowires with mean diameter of 20 nm were synthesized by chemical vapor deposition (CVD) driven bottom-up growth and subsequently transferred via a printing process to Si/SiO_2 chip substrates. Thereby, dense parallel aligned nanowire arrays are created. After dry oxidation of the nanowires, standard photolithography and deposition methods are employed to contact several hundred nanowires with interdigitated Ni electrodes in parallel. A silicidation step is used to produce axially intruded Ni-silicide (metallic) phases with a very abrupt interface to the Si (semiconducting) segment. Acting as front gate dielectric, the chip surface is entirely covered by an Al_2O_3 layer. For sensor applications, this layer further serves as electrical isolation of the electrodes and protects them from corrosion in electrolytes.

Fabricated devices are part of the SOI (Si on insulator) transistor family with top (front) and back gate and exhibit ambipolar rectifying behavior. The top gate exhibits omega geometry with a 20 nm thin Al_2O_3 dielectric, the back gate planar geometry with a 400 nm thick SiO_2 dielectric. The influence of both gates on the charge transport is summarized in the statistical analysis of transfer and output characteristic for 7 different lengths (for each 20 devices) of the Si conduction channel. A nonlinear scaling of on-currents and transconductance with channel length is revealed. Off-currents are influenced from both p- and n-type conduction at the same time. Increasing lateral electric fields (LEF) lead to a decline of suppression capability of both p- and n-currents by a single gate. This is reflected in a deteriorated swing and higher off-current towards decreasing channel lengths (increasing LEF). However, by individual gating of Schottky junction and channel, p- and n-type currents can be controlled individually. Both charge carrier types, p and n, can be suppressed efficiently at the same time leading to low off-currents and high on/off current ratio for all investigated channel lengths. This is achieved by a combined top and back double gate architecture, for which the back gate controls the Schottky junction resistance. It is demonstrated that a fixed high Schottky junction serial resistance, severely impairs the transconductance. However, the transconductance can be significantly increased by lowering this resistance via the back gate, enhancing the transducer performance significantly.

Al_2O_3 covered SB-FETs were employed as pH sensors to evaluate their performance and signal to noise ratio (SNR). Current modulation per pH was observed to be directly proportional to the transconductance. The transistor related signal to noise ratio (SNR) is thus proportional to the transconductance to current noise ratio. Device noise was characterized and found to limit the SNR already below the peak transconductance regime. Statistical analysis showed that the nanowire

SB-FET transconductance and noise both scale proportional with the current. Therefore, the SNR was found to be independent on the nanowire channel lengths under investigation.
The high process yield of nanowire SB-FET parallel array fabrication close to hundred percent enables this platform to be used for simple logic and biosensor elements. Because of the low fabrication temperatures needed, the foundation is laid to produce complementary logic with undoped Si on flexible substrates. For previously reported results, the presence of Schottky junctions severely impaired the transconductance, restricting the applicability of SB-FETs as transducers. This work shows, that an electric decoupling of the Schottky junction can reduce these restrictions, making SB-FETs feasible for sensor applications.

KURZFASSUNG

Diese Dissertation ist der Bewertung von Silizium (Si) Nanodraht basierten Parallelschaltungen von Schottky-Barrieren-Feld-Effekt-Transistoren (SB-FETs) als Wandler für potentiometrische Biosensoren und deren generelle Leistungsfähigkeit als Bauelement neuartiger funktioneller Elektronik gewidmet. In dieser Arbeit wurden Parallelschaltungen von Nanodraht SB-FETs hergestellt und elektrisch charakterisiert. Nominell undotierte Si Nanodrähte mit durchschnittlichem Durchmesser von 20 nm wurden mittels chemischer Dampfphasenabscheidung (CVD) synthetisiert und anschließend durch einen Druckprozess auf ein Si/SiO_2 Chip-Substrat transferiert. Damit wurden dicht gepackte, parallel ausgerichtete Nanodraht Schichten erzeugt. Nach Trockenoxidation der Nanodrähte wurden diese mit Standard Lithographie und Abscheidungsmethoden mit interdigitalen Nickel (Ni) Elektroden als Parallelschaltung kontaktiert. Durch einen Temperprozess bilden sich axial eindiffundierte metallische Ni-Silizid-Phasen, mit einer sehr abrupten Grenzfläche zum halbleitenden Si Segments des Nanodrahts. Die Chipoberfläche wird vollständig mit einer Al_2O_3-Schicht bedeckt, welche als Frontgate-Dielektrikum oder als elektrische Isolation und Korrosionsschutzschicht für Elektroden in Elektrolytlösungen im Falle der Sensoranwendungen dient.
Die hier gezeigten Bauelemente sind Teil der SOI (Si on insulator) Transistoren-Familie mit Top- (Front) und Backgate und zeigen ein ambipolares Schaltverhalten. Die Topgates besitzen eine Omega-Geometrie mit 20 nm dickem Al_2O_3 Dielektrikum, das Backgate eine planare Geometrie mit 400 nm dickem SiO_2 Dielektrikum. Der Einfluss beider Gates auf den Ladungstransport ist in einer statistischen Analyse der Transfer- und Output-Charaktersitiken für 7 unterschiedliche Si-Leitungskanallängen zusammengefasst. Eine nichtlineare Skalierung von Strom und Transkonduktanz mit Leitungskanallänge wurde aufgedeckt. Die Ströme im Aus-Zustand des Transistors sind durch das Vorhandensein gleichzeitiger p- als auch n-Typ Leitung bestimmt. Die Zunahme lateraler elektrischer Felder (LEF) führt zu einem Verlust des gleichzeitigen Ausschaltvermögens von p- und n-Strömen bei Ansteuerung mit einem einzelnen Gate. Dies äußert sich durch einen graduell verschlechterten Swing und höheren Strom im Aus-Zustand bei verringerter Leitungskanallänge (gleichbedeutend mit erhöhten LEF). Durch eine getrennte Ansteuerung von Schottky-Kontakt und Leitungskanal lassen sich p- and n-Leitung jedoch unabhängig voneinander kontrollieren. Beide Ladungsträgertypen können so simultan effizient unterdrückt werden, was zu einem geringen Strom im Aus-Zustand und einem hohen An/Aus- Stromverhältnis für alle untersuchten Kanallängen führt. Dies wird durch eine Gatearchitektur mit kombiniertem Top- und Backgate erreicht, bei der das Backgate den Ladungstransport durch den Schottky-Kontakt und dessen Serienwiderstand kontrolliert. Es wird gezeigt, dass ein konstant hoher Schottky-Kontakt bedingter Serienwiderstand die Transkonduktanz erheblich vermindert. Jedoch kann die Transkonduktanz im höchsten Maße durch eine Herabsetzung des Serienwiderstandes durch das Backgate gesteigert werden. Dies erhöht die Leistungsfähigkeit des SB-FET als Wandler deutlich.

Al_2O_3 oberflächenbeschichtete SB-FETs wurden als pH-Sensoren erprobt, um deren Tauglichkeit und Signal-zu-Rausch-Verhältnis (SNR) zu evaluieren. Die Strommodulation pro pH-Wert konnte als direkt proportional zur Transkonduktanz bestätigt werden. Das Transistor bedingte SNR ist daher proportional zum Verhältnis von Transkonduktanz und Stromrauschen. Bei der Analyse des Transistorrauschens wurde festgestellt, dass dieses das SNR bereits bei einer niedrigeren Transkonduktanz als der maximal Möglichen limitiert. Eine statistische Auswertung zeigte, dass sowohl SB-FET Transkonduktanz als auch Stromrauschen proportional zu dem Transistorstrom skalieren. Somit ist deren Verhältnis unabhängig von der Nanodraht-Leitungskanallänge, im hier untersuchten Rahmen.

Die geringe Ausschuss bei der Fabrikation der Nanodraht SB-FET-Parallelschaltungen ermöglicht eine Nutzung dieser Plattform für simple Logik und Biosensorelemente. Durch die geringen Prozesstemperaturen wurde die Grundlage geschaffen, komplementäre Logik mit undotiertem Si auf flexiblen Substraten zu fertigen. Vorangegangene Resultate zeigte eine verminderte Transkonduktanz durch die Präsenz von Schottky-Barrieren, was die Anwendbarkeit von SB-FETs als Wandler einschränkt. Diese Arbeit zeigt, dass eine elekrtische Entkopplung der Schottky-Kontakte zu einer Aufhebung dieser Beschränkung führen kann und somit den Einsatz von SB-FETs als praktikable Wandler für Sensoranwendungen zulässt.

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ABBREVIATIONS

ALD atomic layer deposition

BioFET field effect transistor based sensor for potentiometric detection of bio molecules

CNT carbon nanotube

FET field effect transistor

GNP Gold nano particle

IE spacing Inter electrode spacing

IES Inter electrode spacing

ISFET ion sensitive field effect transistor

LEF Lateral electrical fields

MIG metal induced gap state

MOSFET metal oxide semiconductor field effect transistor

SOI Silicon on insulator

SB Schottky barrier

SB-FET Schottky barrier field effect transistor

SJ Schottky junction

VLS vapor liquid solid

INTRODUCTION

Nanowires have been in the scope of research for novel unconventional electronics with enhanced functionality during the last decade [1–11]. It is believed that their scalability and high surface to volume ratio will contribute to improved device performance in sensor and electronic applications. During this thesis, bottom-up grown silicon (Si) nanowire Schottky barrier field effect transistors (SB-FETs) were fabricated and characterized with respect to their applicability for biosensors and future electronic building blocks. Bottom-up growth of nanowires is one method to achieve nanometer dimensions which are below the minimum feature size of optical lithographical methods of top-down fabrication [12–15]. Axial and radial heterostructures with multilayer shells can be grown by (catalytic) chemical vapor deposition (CVD) in changing the gas composition and growth parameters during the process [16–19]. This allows for instance to create trillions of nanowires with surround gate stack in a single process step [20, 21]. Although being potentially a low cost alternative to top-down fabrication methods like e-beam lithographical patterning, bottom-up technology is not found in industrial device processing. The crucial drawback of bottom-up synthesis is the lack of positioning control. At some point bottom-up grown nanostructures have to be integrated into a top-down processed device architecture. But controlled assembly on substrates poses technological difficulties. Attempts were made to grow nanowires directly in place on the actual chip at predefined positions with questionable success [22]. Most approaches aim to perform growth on a sacrificial substrate and transfer the nanowires after growth to another chip, followed by self assembly [23–26]. The unguided placement mainly allows to create simple patterns and suffers from large statistical alignment errors and a low yield. Especially for positioning of large numbers of transistors with low margin of error, bottom-up technology is not feasible. Nevertheless, for applications with lower requirements on ordering perfection and device to device variations, this technology appears attractive. Such applications could be flexible electronics and sensor applications with low transistor density. Semiconductor manufacturing involves high temperature processes which

a polymer cannot sustain. The possibility of bottom-up technology to transfer monocrystalline semiconductor materials to flexible substrates after fabrication solves this problem and thus poses a notable benefit.

Especially silicon nanowire transistors are intensely investigated for utilization as future potentiometric biosensors since 2001 [27–34]. They target on the emerging field of point of care diagnostics. One of the visions are portable devices for daily use at home to monitor the health of the consumers. For certain applications health monitoring devices are already commercially available although based on a non-nanowire technology. Diabetes patients use hand held devices to regulate their insulin level [35–37]. To perform the test, the patient takes a blood droplet sample by himself, volumes are around $10\,\mu$l. Glucose levels are very high in blood (4-8 mmol/l) so quantification is unproblematic [38]. However, diagnostics of diseases in an early stage involves very low concentrations ($\sim 1e^{-15}$ mol/l) of bio molecules which requires extremely sensitive devices. A concrete possible field of application would be sensor devices for an instant survey on the norovirus, which was responsible for diarrhea epidemics in hospitals with even lethal consequence in the past [39]. Such a fast test could help to take effective measures in isolating infected patients and containing the epidemic.

A large class of biodetection methods rely on specific binding of the analyte target molecule, e.g. the virus in the previous example, to a receptor molecule [40]. The latter is represented by a wide range of the biomolecules, i.e. antibodies, enzymes, dna and rna strands and their derivatives, e.g. aptamers (short single stranded DNA segments) [41–43]. They are characterized by a high binding affinity specifically to the target molecule. Binding of the analyte target to the receptor immobilized at the sensor surface leads to property changes of the sensor element which are transduced to electrical signals. In sensor systems like surface plasmon resonance (SPR) [44], fluorescent switchable DNA modified surfaces [45], quartz microbalance [46] and cantilever sensors [47], optical or mechanical properties are modified by target molecules. However, large molecule quantities are needed to inflict sufficient property changes for detection and noise multiplies by the transducing cascade to the final electrical signal. Promising competitive systems are field effect transistors, so called BioFETs, for a direct electrical detection of bio molecules. The idea of BioFETs goes back to the ion sensitive field effect transistor (ISFET) reported by Bergveld in 1970 [48]. In short, a concentration gradient of charged species is build up at the electrolyte/gate oxide interface by chemical reactions which generates a surface half-cell potential. The reaction is the receptor/analyte binding for the biosensor or (de)protonation of amphoteric functional groups for the pH sensor. The generated half-cell potential gates the transistor. The current modulation or the shift of threshold voltage is measured which is interrelated with the analyte target concentration of interest. A variety of nano-sized transistors, including CNTs, silicon and other semiconducting nanowires have been reported for potentiometric measurement of bio molecules [27, 49–53]. Due to their scalability, transistor based sensors can be downsized to dimensions comparable to bio molecules in contrast to other sensors. A few molecules bound to the surface are therefore enough to derive significant

signal to noise ratios (SNR). In this class of sensor, silicon nanowires gathered great attention during the last decade. They can be integrated into conventional Si technology and the massive knowledge about chemical modification of oxide surfaces facilitates receptor immobilization. For its high quality Si/SiO_2 interface with a very low defect concentration, Si is the standard material used today in semiconducting industry. The low defect density minimizes charge trapping related transistor noise. Silicon nanowire sensors were demonstrated to be potentially capable to detect single charges [54, 55]. By multiple sensor elements on a chip with different individual receptors immobilized at the surface a differentiation between bio molecule species is possible [56, 57]. This was demonstrated by a multiplexed detection of cancer markers [58]. The capability to produce sensor arrays for multiplexed detection is an important feature which distinguishes the transistor technology from others in terms of feasible and low cost implementation. Fully integrated transistor based sensor device arrays have been demonstrated already [59–62].

For a homogenous and constant surface potential over the entire gate oxide, the SNR is proportional to the ratio of transconductance and current noise [63]. For a good transducer this ratio has to be optimized and is generally regarded to be limited primarily by 1/f transistor noise [64–68]. Indeed, it was experimentally observed that the maximum SNR does not appear at the peak transconductance for nanowires, CNT transistors and conventional MOSFET based ISFETs [66, 69, 70]. Some groups even claim the subthreshold to be the regime with highest SNR [71]. Although at the peak transconductance the current modulation and thus signal is highest, the low frequency noise diminishes the SNR in this regime. The noise characteristics of the specific device will determine the optimal regime for sensing the transistor should be operated in.

However, a good transconductance to noise ratio is not the only criterion to reduce the detection limit. The charge of biomolecules is screened within the Debye length which is 1-50 nm in solution for physiological ionic concentrations [72]. The screening reduces the impact of the molecule charge [73]. Therefore the receptor should be chemically engineered to bring the analyte target as close to the surface as possible to maximize the effect. The radius around the analyte target, where the surface potential is effectively affected, is proportional to the Debye screening length too. Since nanowires exhibit similar diameters like the Debye screening length, almost all the nanowire cross section is affected by a single adsorbed bio molecule. This is the common justification for the employment of nanowires in biosensors. The situation is depicted in figure 1. Still under debate is how big the BioFET transistor should really be. Nanowire hardliners insist on the necessity to downsize the nanowire dimensions comparable to the Debye screening length. However, it was reported that a higher SNR can be achieved with larger transistors [74]. The plausible explanation for this observation is that uncorrelated noise, created at the surface, is gradually averaged out according to the Gaussian propagation of uncertainty when increasing the surface area. The sensor signal scales proportionally to the active sensor area but the noise components add root mean square and thus scales only with the square root of the sensor area. The same considerations are valid for a parallel array of nanowires with small diameter. For N nanowires incorporated into a device, one

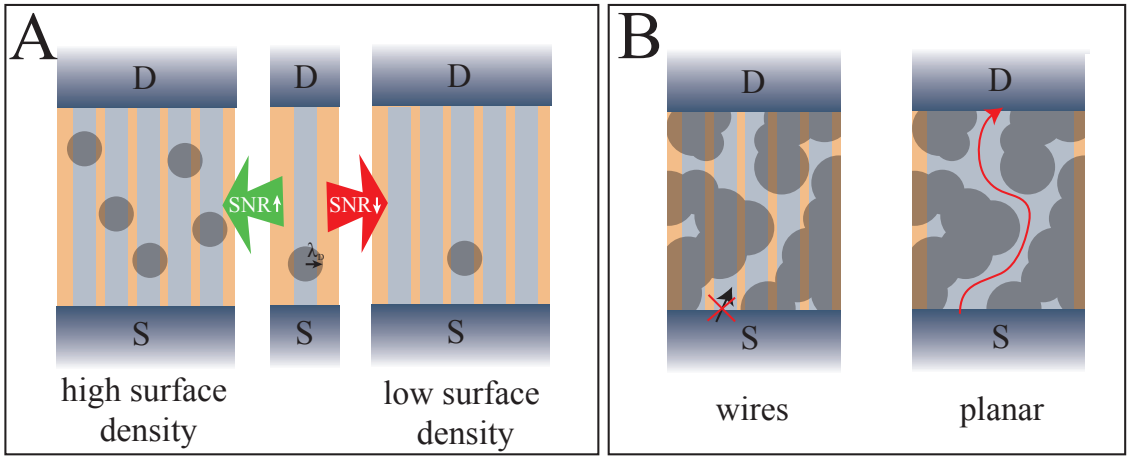

Figure 1: Conception of nanowires parallel arrays for feasible biosensors. A) A target molecule bound to a nanowire (middle) modulates the current between source (S) and drain (N). The radius of the area affected by the molecule is proportional to λ_D (grey discs). An SNR > 1 can be achieved for single nanowires, when a single molecule occasionally binds exactly on the nanowire surface. For a high surface density, a parallel array of nanowires increases the SNR by $\sqrt{N}$. For a very low surface density most nanowires are not influenced by a target but only contribute to noise. In this case the SNR might drop compared to a single nanowire device. B) For the same sensor area parallel arrays of nanowires are expected to improve the SNR compared to a planar FET geometry due to avoidance of percolation paths.

expects the SNR to increase by $\sqrt{N}$. This would imply to make the sensor area as big as possible to increase the SNR. This is also valid for an irregular occupation of the surface with target molecules which leads to an inhomogeneous modified surface potential. Further, a parallel array of nanowires will probably be able to modulate the current more efficiently compared to a planar transistor with the same sensor surface area. The uniaxial charge transport in nanowires prohibits percolation paths which can develop in planar BioFET sensors for an inhomogeneous surface potential [75]. However, a large sensor size might not be capable of very low surface molecule and thus low charge densities. For the targeted concentrations, the target molecules can be spatially separated by several micrometers on the sensor surface. It seems even questionable whether the half-cell potential can arise for these small surface charge densities at all. For such low surface densities many nanowires might not exhibit adsorbed targets on their surface and will only contribute to the noise level. The SNR of the nanowire array will then be substantially smaller compared to a single nanowire with bound molecule. Detection of single or very few molecules might therefore only be possible with single nanowires. The described dilemma suggests, there might exist different optimum sensor sizes depending on the concentration range to be measured. However, the probability of a single molecule binding exactly to the small surface of a single nanowires is small though. This high uncertainty raises doubts about the feasibility of single nanowire devices in realistic applications. Therefore parallel arrays of nanowires have been proposed as sensor devices [76].

The aim of this thesis was the development, fabrication and characterization of bottom-up grown nanowire transistors for sensor and functional electronic applications. Nanowire transistors were implemented as Schottky barrier field effect transistors (SB-FET) with axially intruded $NiSi_2$ metallic contacts which were reported before [77–79]. The $NiSi_2$ phase shows a very smooth and up to atomically abrupt interface to the silicon (Si) part of the nanowire. This leads to very homogenous and reproducible Schottky barrier heights in contrast to bulk SB-FETs with arbitrary NiSi phases [80]. The metallic $NiSi_2$ segment, intruded into the nanowire, leads to an electric field enhancement at the needle-shaped tip. This increases the Schottky barrier thinning beyond the subthreshold regime leading to an accelerated transition to the transistor on state. Such devices show ambipolar transfer characteristics when operated by a single gate. By a dual gate architecture a reconfigurable transistor is generated which can switch operation mode from unipolar p- to n-type during runtime [11, 81–83]. This enhanced functionality could replace the two CMOS logic building blocks (p-and n-type transistors) by a single one in nanowire SB-FET electronics. For such devices it was shown that the current modulation happens at the very localized region of the Schottky junction beyond the subthreshold regime by controlling the tunneling barrier [84]. Therefore, small amounts of charges are considered to be sufficient to gate the transistor. This could increase the charge sensitivity, which is an interesting feature for biosensor applications. Despite, for CNTs the importance of the Schottky barrier contacts is often discussed for sensing and sometimes is claimed to be the most sensitive location [49, 85].

In this thesis the feasibility of nanowire SB-FETs should be assessed for ISFET and biosensing applications. Another novelty of this particular thesis was to produce parallel arrays of those SB-FETs which can be employed as noise resistant transducers with enlarged SNR. Single nanowire SB-FET devices with intruded $NiSi_2$ contacts were the technology being available at the beginning of this thesis. Since those devices exhibit still very high resistivity in the on state ($1\,M\Omega$) an assembly in parallel arrays was targeted to amplify the output currents. The main innovations and improvements which were required to achieve a feasible and reliable transistor platform for ISFET technology were:

1. increase device yield and device-to-device variations by creation of parallel arrays nanowires with improved diameter uniformity
2. establish deposition method for high density arrays of nanowires with defined orientation
3. optimize transistor to achieve high current densities together with a high on/off current ratio and high transconductance
4. create a new chip design for which sufficient nanowires can be contacted simultaneously and a microfluidic channel can be integrated on the chip
5. find a passivation strategy which prevents ion diffusion and electrochemical degradation of the electrodes
6. reduce the charge trap density and related effects degrading the electrical performance

The augmented output current should guaranty a high tolerance against external noise sources during readout. Additionally, the incorporation of multiple nanowires into a transistor structure leads to an increase of process yield and reduces device to device variations. Besides, the parallel assembly approach allowed to extract vast statistical data on the nanowire SB-FET device performance. Furthermore, the high fabrication process yield close to hundred percent enables potentially on chip (reconfigurable) logic for simple signal processing on rigid and flexible substrates without the need for further process optimization.

Chapter 1 introduces the reader to transistor theory in general, including a comparison between MOSFET and SB-FETs and the working principle and noise sources in ISFETs. Fabrication of parallel array nanowire SB-FETs and chip design are discussed in detail in chapter 2. The platform was electrically characterized with regards to transfer, output and noise characteristics. The results including trends in transconductance to current noise ratio are given in chapter 3. Those trends were compared with the SNR obtained in pH sensing experiments. The pH sensor applicability was verified by sensor response tests on pH samples, presented in chapter 4. Finally, the effect of the Schottky barriers on the transconductance and transducer capabilities of the presented platform are discussed in chapter 5. By an electrostatic decoupling of the Schottky juntions to the electrolyte and front gate, their influence on the current modulation was assessed. Furthermore, a double gate approach with back and front gate led to a parallel array of reconfigurable transistors. A summary and outlook for this transistor type as platform for biosensorics and future electronic applications with enhanced functionality is discussed in chapter 6.

1 FUNDAMENTALS

In this chapter the reader is introduced to the fundamentals of nanowire growth, transistor theory and pH and biosensing. Furthermore, the charge transport in silicon nanowire Schottky barrier field effect transistor (SB-FETs) is explained and differences to conventional MOSFET technology are discussed.

1.1 BOTTOM UP GROWTH OF SI NANOWIRES

Particle assisted bottom up growth of Silicon nanowires (whiskers) and VLS mechanism was first described by Wagner and Ellis 1964 [86]. Originally regarded as a side effect of undesired metallic contaminants, it was exploited amongst others for electronic sensor research by the group of Charles Lieber in the early nineties [87]. The growth can be performed in a CVD (chemical vapor deposition) furnace. CVD is usually used to deposit layers of materials by thermal decomposition of a so called precursor gas on a heated surface. An example is silicon deposition with SiH_4 (silane) as precursor at temperatures of 650-800 °C [88]. The basic idea of nanowire growth is to decrease the process temperature to a level below (or around) the thermal decomposition (420 ^{0}C) of the precursor. Primarily at the surface of metal particles on the growth substrate, the gas is reduced by a catalytic reaction [14]. Au is commonly used as seed particle. Alternative catalyst particles for VLS growth are not easy to find. The eutectic has to have a lower melting temperature than the thermal decomposition T of precursor. The phase transition line has to neighbor the pure Si phase, so that precipitated material (the nanowire) is pure Si and not an alloy of Si and catalyst material. Additionally, the Nebolsin stability criterion has to be fulfilled. The eutectic diagram of the Au-Si system is shown in figure 1.1 reproduced from [14]. Silane SiH_4 was used in this work

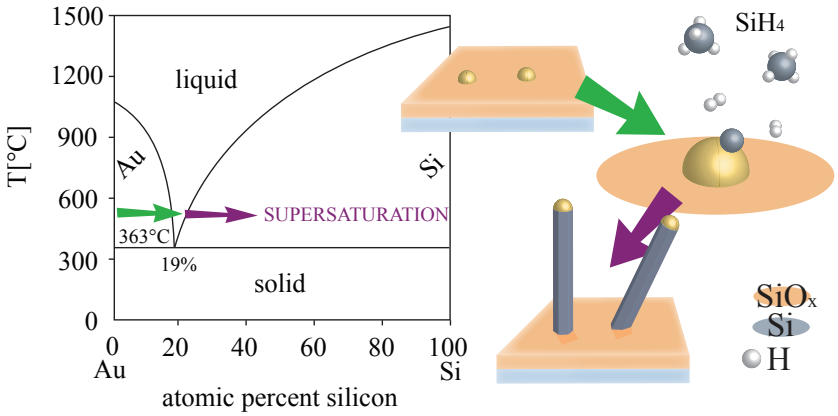

Figure 1.1: VLS (vapor liquid solid) growth mechanism of silicon (Si) nanowires and Au-Si eutectic diagram: during growth via VLS mechanism, the vapor, i.e. silane, is catalytically cracked at the Au particle at T>363 ^{0}C. Si enriches in the particle until the liquidus line is passed. The AuSi droplet melts. As the AuSi droplet gets oversaturated with Si, the excess Si precipitates under the droplet to form a nanowire.

as precursor which decomposes in the following reaction:

$$SiH_4 \rightarrow Si + 2H_2 \tag{1.1}$$

The produced H_2 gas escapes into the chamber, the Si content increases on the seed particle surface. The Si content increases until the liquidus line is exceeded. The particles melt to form an AuSi eutectic mold of liquid droplets. The droplets are further enriched with Si until it is oversaturated when crossing the liquidus line for the second time. The excess Si crystallizes at the bottom of the Au particle. As the Si layers grow at the bottom, the AuSi droplet is continuously lifted. The nanowires grow vertically on top of the substrate with the AuSi particle remaining on the nanowire tip. Since the silicon undergoes a transition from gas to liquid and then to the solid phase the growth mechanism is called VLS (vapor, liquid, solid). Interestingly, grown nanowires were shown to have a monocrystalline structure with a low defect density [87, 89, 90]. The crystal orientation was reported to vary with every process parameter (chamber pressure, partial pressure of the gases, temperature, flow rate) and with the nanowire diameter [13, 14, 87, 91]. The latter is resulting from the surface Gibbs free enthalpy to volume Gibbs free enthalpy ratio being dependent on the nanowire diameter. Growth theory suggests that there can be even plenty of crystal orientations for one specific seed particle diameter because of thermodynamical fluctuations and experiment approved this prediction [92]. Au is marginally incorporated into the silicon and remains on top of the silicon nanowire, so growth can be continued until the desired nanowire length is obtained without changing the morphology or crystal structure. Au is a contaminant which has to be avoided since it generates mid gap states in the Si band gap which promote to charge carrier recombination [14, 93]. However, studies revealed the possibility of small Au incorporation into the nanowire creating deep charge traps [94, 95].

1.2 MOS AND SCHOTTKY BARRIER TRANSISTOR THEORY

In this chapter we review the main aspects of transistor operation and how ISFETs are employed to measure electrochemical potentials. The difference of MOSFET and SB-FETs, bulk and SOI structures like nanowires will be pointed out and discussed which system seems to be optimal for sensor operations. Further, the reader is introduced to charging effects which lead to noise and drifts and thus reduce the signal to noise ratio.
The reader is referred to other publications for a detailed description of the working principle of MOSFETs and transistor basics [96–100]. Here, we emphasize most important aspects which will be important for discussion and comparison between common Si based MOSFET and SB-FET technology. All transistor types have in common the existence of energy barriers for charge carrier transport across the conduction path which can be modulated by external applied voltages at the gate. With the energy barrier modulation the resistance of the transistor changes. However, the origin of energy barriers are fundamentally different for MOSFETs and SB-FETs and lead to different appearance of the transfer characteristics.

1.2.1 MOSFET: Metal Oxide Semiconductor Field Effect Transistor

For MOSFETs charge carriers travel in the same crystal when passing the junctions. Energy barriers are artificially engineered by the doping profile across the conduction path. A potential difference, i.e. energy barrier, builds up at the pn and np junctions due to charge carrier diffusion. At the thermal equilibrium, when Fermi levels align across the junction, this built-in potential is:

$$\Phi_{np} = \frac{1}{e}(E_{Fn} - E_{Fp}) = \frac{kT}{e}\ln(\frac{N_d N_a}{n_i^2}) \tag{1.2}$$

with E_{Fn}, E_{Fp} being Fermi energies in n and p-doped region, e elementary charge, kT Boltzmann constant times temperature, n_i the intrinsic charge carrier density. The built-in potential is thus dependent on the doping concentration of acceptors N_a and donors N_d in p and n-region respectively. The resulting energy barrier can be completely levelled by compensating the built-in potential Φ_{np} by the gate voltage V_g. In this case, at the so called threshold voltage V_{th}, the transistor turns on. How far the source/drain current I_{sd} is affected by the gate voltage V_g is represented by the so called transfer characteristics. The convention for the terminology is $I_{sd} = I_s - I_d$ and $V_{ds} = V_d - V_s$. In the following, source voltage will be defined as $V_s = 0V$, the gate to source voltage V_{gs} will be denounced as V_g. The channel potential Φ_{ch} is defined as the electric potential at the interface of semiconductor and gate oxide in the middle of the conduction channel between source and drain.
A field effect transistor (FET) can be regarded as a serial resistance of junctions R_s, R_d and conduction channel R_{ch} which all vary with V_g. The energy band situation is shown exemplarily for

a npn-MOSFET in figure 1.2 for transistor operating regimes below (subthreshold) and beyond V_{th}. In the subthreshold regime, when the junction resistance R_s is much higher than the channel resistance R_{ch}, V_{ds} drops over the junctions. The potential inside the channel is almost flat since charge carriers can redistribute to screen the electric fields within the depletion width W_D (space charge region). Charge transport happens via diffusion rather than drift. The channel potential Φ_{ch} can be modulated by V_g with the proportionality factor κ, called the gate coupling, where $\delta\Phi_{ch} = \kappa\delta V_g$. To obtain a high gate effectiveness, κ has to be close to one. Charge carriers with energies E higher than the modified energy barrier $e\Phi_{np}^{eff} = e(\Phi_{np} - \delta\Phi_{ch})$ can pass from source to drain. The source/drain current I_{sd} increases exponentially as the energy barrier is lowered with V_g in the subthreshold regime below V_{th}:

$$I_{sd} \simeq I_0 e^{-e\Phi_{np}^{eff}/kT} = I_0 e^{e\kappa(V_g - V_{th})/kT} = I_0 10^{(V_g - V_{th})/S} \tag{1.3}$$

$$S = \frac{1}{\kappa}\frac{kT}{e}\ln(10) = \frac{1}{\kappa}59\text{mV/dec}\frac{T[K]}{300} \tag{1.4}$$

where S is the so called subthreshold swing (invers subthreshold slope), which is limited to 59 mV/dec[1] for $\kappa = 1$ at room temperature. The subthreshold slope SS = 1/S will be defined as $\partial\log_{10}(I_{sd})/\partial V_g$ in this work.

Beyond V_{th} the junction resistance is essentially nulled and the channel resistance R_{ch} dominates the transistor. V_{ds} drops inside the channel from drain to source, charge carrier transport is by drift. The channel potential Φ_{ch} can now hardly be modulated further by the gate voltage V_g ($\kappa_g \to 0$) since (inversion) charge injected from the contacts can accumulate according to V_g inside the channel to screen the gate fields. For $V_g > V_{th}$ it follows:

$$Q_{ch} = (V_g - V_{th})C_{ox} \tag{1.5}$$

$$I_{sd} \simeq \frac{W}{L}Q_{ch}\mu V_{ds} = \frac{W}{L}(V_g - V_{th})C_{ox}\mu V_{ds} \tag{1.6}$$

with μ the mobility of the (inversion) charge carriers, W width and L length of the conduction channel. Not an energy barrier, but the oxide capacity C_{ox} limits the charge in the channel Q_{ch} and therefore I_{sd}. I_{sd} increases direct proportional to V_g. Therefore this transistor regime is often called linear regime. For large V_g the linear increase of I_{sd} stops because scattering in the channel limits the conductivity. The current modulation with V_g is called transconductance $g_m = \partial I_{sd}/\partial V_g$ and is:

$$\partial I_{sd}/\partial V_g = \frac{W}{L}C_{ox}\mu V_{ds} \tag{1.7}$$

in the linear regime. For $V_g < V_{th}$ the transconductance is dependent on κ.

[1] This is also called the Nernstan slope and appears always when electrical fields counter thermally driven motion of charged species in a concentration gradient.

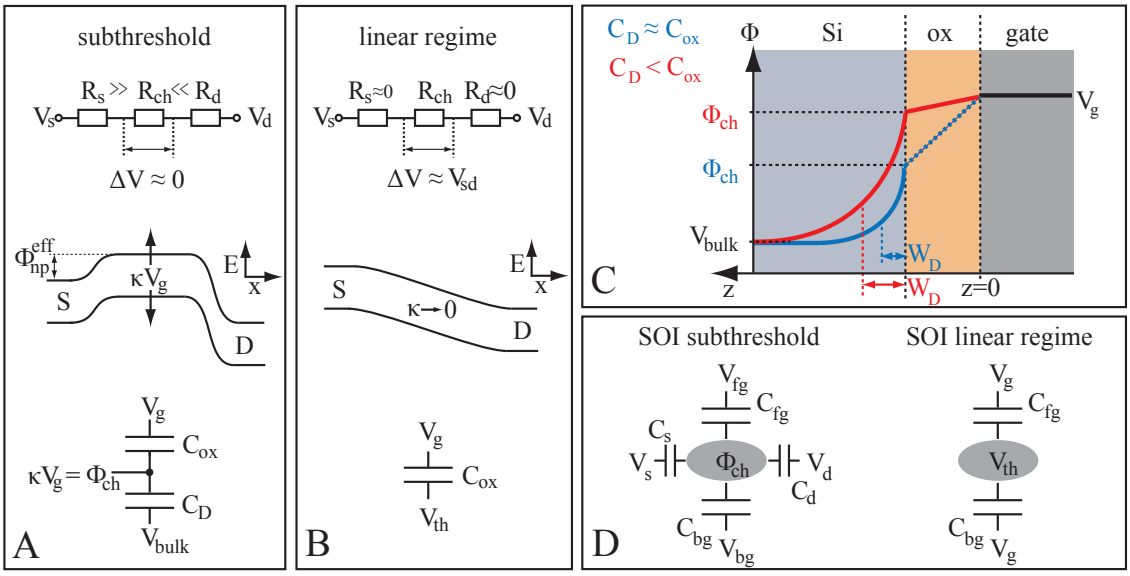

Figure 1.2: Energy band profiles and voltage divider analog circuits in different transistor working regimes: A) Subthreshold regime for MOSFETs with neglectable source/drain influence on channel potential Φ_{ch}. Gate coupling κ is determined by depletion layer capacitance C_d and gate oxide capacitance C_{ox}. Electric potential Φ from source to drain (x-direction) is almost constant, energy bands are flat. The current is limited by the energy barriers at source and drain. B) In linear regime, the electric potential decays from source to drain within the channel. The current is limited by C_{ox}, since it limits the (inversion) charge $Q_{ch} = (V_g - V_{th})C_{ox}$ in the channel. C) Electrical potential Φ profile from gate to bulk (z-direction) for small and large C_{ox}/C_d ratio, i.e. κ. D) Analog circuits for silicon on insulator (SOI) devices with source, drain and back gate influence on Φ_{ch}. Voltage divider circuits are used for approximation of κ in subthreshold and channel charge Q_{ch} in linear regime.

1.2.2 Gate coupling

The gate coupling κ determines how effectively the vertical electric fields (z-direction) can penetrate the Si channel. The situation is depicted in figure 1.2C. Part of the applied gate to bulk voltage drops over the gate oxide. The potential at the Si/oxide interface under the gate oxide, here called the channel potential Φ_{ch},[2] decays exponentially in the bulk (z-direction) because of charge carrier screening. The characteristic length for which the potential dropped to 1/e Φ_{ch} (e is the Euler number) is called the screening length, or depletion width W_D. Φ_{ch} can be approximated by using a voltage divider analog circuit between the gate oxide capacitance C_{ox} and the underlying depletion layer capacitance C_D. C_{ox} and C_D are connected in serial, one side connected to V_{bulk} (for simplicity here assumed to be zero) and the other to the gate terminal voltage.

$$\delta\Phi_{ch} = \kappa\delta V_g \tag{1.8}$$

$$\kappa = \frac{C_{ox}}{C_D + C_{ox}} \tag{1.9}$$

[2]The term often found in literature for the potential at the Si/oxide interface is surface potential. However, one likes to reserve the term surface potential to the sensor surface in this work. To avoid confusion the terminology differs here from the common one.

So a high ratio of oxide capacitance to depletion layer capacitance C_D is preferred for high gate effectiveness. The voltage drop over the oxide is consequently (1-κ)δV_g. C_D is indirectly proportional to the depletion width $C_D = \epsilon / W_D$ and is thus varying with the charge carrier concentration. In the linear regime (strong inversion), when a lot of inversion charge is present in the channel, C_D is strongly increased. The gate coupling κ drops to zero. The band bending is not steered anymore by V_g, but only the inversion charge accumulation.

For SOI (silicon on insulator) devices, like the Si nanowire FETs presented here, the bulk is not electrically connected to the channel. However the bulk affects the channel potential from the back side. The bulk for SOI is therefore called back gate, separated by the BOX (buried oxide) or back gate oxide from the channel. For a thick SOI (partially depleted) two depletion layers form at the back and front gate oxide surface. There are essentially two conduction channels formed independently by two gates. The back gate controls the back side and front gate controls the front side separately. If the Si thickness between front and back gate oxide is thinner than the depletion width W_D the SOI is called fully depleted. For full depletion, C_D does not exist in vertical direction. Since the dimensions are limited in vertical direction, no screening can take place in vertical but only in longitudinal direction. The channel potential is hardly varying in vertical direction. Φ_{ch} is modulated by all terminal voltages. The terminals are source, drain, front gate and back gate for SOI-FETs. How far the terminal voltages affect Φ_{ch} can be approximated with a capacitive voltage divider analog circuit visualized in figure 1.2D [4].

$$\delta\Phi_{ch} = \sum_{i=1}^{n} \kappa_i \delta V_i \tag{1.10}$$

$$\kappa_i = \frac{C_i}{\sum_{j=1}^{n} C_j} \tag{1.11}$$

where C_i are capacitances and V_i the potential of the individual terminals. The coupling factors κ_i sum up to one. A δ is written in the formula, to take into account that Φ_{ch} is also influenced by constant built-in potentials. The gate voltage drops over terminal capacitances with low coupling. For a high gate coupling, the electric fields are therefore built up mainly laterally over source and drain when V_g is raised. Φ_{ch} is varying from source to drain (along the x-direction), depending on the local capacitive influence of the terminals, the charge carrier density and mobility. The energy band progression in x-direction will generally be an intermediate case between the two idealized cases depicted in figure 1.2A for the subthreshold and linear regime. For the sensor device, the front gate terminal voltage is affected by the analyte target reaching the surface. The device should therefore be maximally influenced by the front gate. For gas sensors the front oxide is exposed to the analyte gas. In this work, the front gate is exposed to the ambient air in case of the back gated devices. The front gate terminal voltage can be determined by a metal top gate or by a combined

electrolyte-reference-electrode in case of the sensor. In sec. 3 the impact of the gate coupling on the transfer characteristics is presented.

1.2.3 Oxide charges and flatband voltage

The discussed built-in potential Φ_{np} of the np junction leads to lateral electrical fields from source to drain, here defined as x-direction. Commonly, vertical electrical fields from gate to bulk (z-direction) are built-in as well. Si bands are therefore already bent for unbiased gate voltage. The so called flatband voltage V_{FB} is the gate voltage, for which the Si energy bands under the gate dielectric are not bent (in z-direction). At $V_g = V_{FB}$, the channel is free of vertical electrical fields and there is no charge accumulation or depletion. The reason for vertically built-in electric fields are charges in the gate oxide and the work function difference between gate and the Si channel Φ_{ms}. Since the work function of gate material and semiconductor (channel) are likely to differ, charge will redistribute from gate to channel until their Fermi-levels match. Oxide charge, modifying V_{FB}, is categorized in fixed charge Q_f at the Si/oxide interface which is generated during fabrication process, interface trapped charge Q_{it}, oxide trapped charge Q_{ot} and mobile ionic charge Q_m. Q_{it} is reversibly trapped at the Si/oxide interface for a characteristics period (charge trap lifetime) and can lead to a change of V_{FB} over time. However, depending on the charge neutrality level, discussed in section 1.2.4, charge Q_{it} is trapped at the interface in thermal equilibrium. This charge can be detrapped during device operation. Q_{ot} is trapped charge distributed within the gate dielectric. Deeply trapped Q_{ot} can be generated for instance by injection of hot electrons. Q_m are ions which are incorporated in the gate dielectric during device fabrication. Depending on temperature and electric fields strength in the oxide, they are able to redistribute within the oxide. Charges in the insulating gate dielectric will be screened from either channel or gate side. If charges are close to the Si/oxide interface ($z = t_{ox}$), counter charge will accumulate in the channel to screen the oxide charges, leading to a modification of V_{FB}. Charges present at the gate side (at $z = 0$) are screened by image charges in the gate. Thus they do not affect the potential inside the transistor channel and V_{FB}, if the gate is metallic. The flatband voltage V_{FB} is given by [100]:

$$V_{FB} = \Phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}}{C_{ox}} - \int_0^{t_{ox}} \frac{z}{t_{ox}} \rho_m(z)\,dz - \int_0^{t_{ox}} \frac{z}{t_{ox}} \rho_{ot}(z)\,dz \tag{1.12}$$

where ρ_m is the charge density of mobile ionic and ρ_{ot} of oxide trapped charges, t_{ox} the thickness of the gate dielectric and $z = 0$ at the gate/oxide interface. The threshold voltage V_{th} is shifted by the flatband voltage V_{FB}. Depending on V_{FB} devices are turned on or turned off at $V_g = 0V$. These cases are referred to as normally-on or normally-off, respectively. In case of a polarizable gate, which applies for the liquid gate (electrolyte) in the biosensor, charges at the gate side are partly screened from the gate and channel side additionally. Therefore, charges at the dielectric/liquid gate interface ($z = 0$) do affect V_{FB}.

1.2.4 Charge trapping and charge-voltage hysteresis

During device operation, charge can be reversibly captured inside or at surfaces of the gate oxide. This phenomenon is called charge trapping and shifts the flatband voltage (and thus V_{th}) for a limited period or permanently. Charge can be injected into localized energy states via tunneling or thermally [101, 102]. The occupation/vacation rate of trap states depends on the tunneling distance and the activation energy. Both can be altered by the potential drop over the oxide. For a low κ, the potential difference over the oxide $\delta V_g - \delta\Phi_{ch} = (1-\kappa)\delta V_g$ increases strongly. For traps which are deep inside the oxide, charge trapping is promoted then. Charge trapped deeply in the oxide is often not easily released and exhibits a large retention time. Charge trapped directly at the Si/oxide interface is called interface trap charge Q_{it}. At these interface states, charge is easily trapped and released leading to short trap lifetimes τ_{it} and a fast reaction on external voltage bias changes [103]. Since they are close to the conduction channel their impact on V_{FB} is large as can be seen from equation 1.12. Charge traps occur at interfaces because of lattice mismatches of two materials [104]. Uncoordinated Si bond, called dangling bonds, are amphoteric, which means they pose a charge trap for electrons and holes. Those bonds can provide or accept an electron. The density of interface states D_{it} and their energy distribution depends on the combined materials and crystal orientation. The Si/SiO_2 (100) interface has a very small D_{it} and an energy distribution symmetric to the middle of the Si band gap [105]. This means, there exist the same amount of traps for holes and electrons, which is important for complementary logic. Therefore Si (100) planes are used in semiconducting industry as gate oxide stack interface. Nanowires exhibit a variety of Si surfaces which might show asymmetric and larger D_{it}, like for instance the Si (111) plane [87, 90]. Up to which level interface states are occupied in thermal equilibrium is described by the charge neutrality level (CNL) [106–110]. It can be regarded as the Fermi energy of the interface isolated from the bulk. For a large D_{it} and low doping concentration, the Fermi level at the surface is pinned at the CNL [111, 112]. Depending on doping concentration and CNL, charge redistributes between interface and bulk and Si bands are bent at the interface in the unbiased case [113]. For instance, a CNL in the Si band gap middle and n-type Si would result in charge transfer of electrons into interface states and therefore an upward bending of Si bands at the interface. Nominally undoped Si with E_F in the middle of the band gap and a CNL of interface states below E_F would lead to electron injection into the surface states and hole accumulation in the semiconductor. For undoped Si, the charge carrier density is so low that even for low D_{it} one might find the surface potential determined by the CNL.

Under voltage bias, the interface states are occupied according to the potential at the Si/oxide interface (Φ_{ch}). Q_{it} accumulates generally with a certain time delay, related to $R_{it}C_{it} = \tau_{it}$, called interface trap lifetime. When charge accumulates in the Si channel due to applied V_g it can either be trapped or conduct current. Therefore, trapped charge accumulation can be modeled as capacitance $C_{it} \sim D_{it}$ in parallel to C_D [97, 100]. For high frequency sweeping $f >> 1/\tau_{it}$ of V_g,

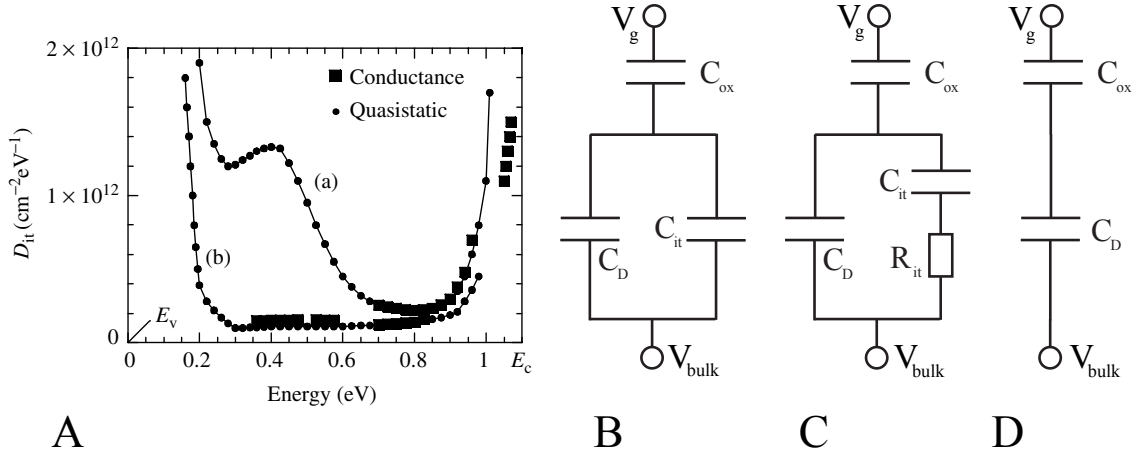

Figure 1.3: Charge trapping caused by Si to gate oxide interface states: A) Density of interface charge trap states D_{it} at a) n-Si <111> and b) n-Si <100>from [100]. B-D) Charge trapping analog circuits: B) low frequency limit, C) intermediate frequencies, when hysteresis is observed in transfer characteristics, D) high frequency limit. Charge trap lifetime τ_{it} is given by $R_{it}C_{it}$. Analog circuit can be applied as well for charge traps within the bulk of the oxide, exhibiting high R_{ot} and long lifetimes τ_{ot}.

trapping is not fast enough to follow the driving force (figure 1.3). For low frequencies $f << 1/\tau_{it}$ all traps of energy states up to the Fermi level will be occupied. The gate coupling is then lowered by C_{it}:

$$\kappa = \frac{C_{ox}}{C_D + C_{ox} + C_{it}} \tag{1.13}$$

Therefore, charge trapping degrades κ and consequently the subthreshold slope. In the intermediate frequency case, there is a phase lag between Q_{it} and V_g, resulting from the $R_{it}C_{it}$ resonant circuit. This manifests in the transfer characteristics (I_{sd} vs. V_g) as hysteresis. Depending on the V_g sweeping frequency, charge-voltage hysteresis and degradation of the subthreshold slope happen simultaneously. Generally, interface charge traps at the Si/SiO_2 interface have very short lifetimes (τ_{it} ~1-10 μs) and lead to a degradation of κ rather than hysteresis for the low frequency regime (0.1-10 Hz) [103]. Hysteresis, observed on timescales of milliseconds up to minutes and hours, is associated with charge, tunneling reversibly into oxide trap states close to the Si/SiO_2 interface within the bulk of the oxide [101, 103, 114, 115]. These traps are thus often called deep or slow traps. Nevertheless, the analog circuit depicted in figure 1.3 can be applied for oxide charge traps too, substituting R_{it}, C_{it} with R_{ot}, C_{ot}. If the rates of trapping and detrapping deviate from each other, $R_{ot}(V)$ is voltage dependent. For such a case, this leads to a more complicated time dependency of charge trapping which can not represented by a simple RC analog circuit. A possibility to avoid hysteresis during measurements, is applying V_g in pulses (pulsed measurement) to minimized charge trapping and allow charge detrapping during the pulse off period. Despite, charge-voltage hysteresis in MOS transistors can be caused as well by mobile ions [116] and dielectric or interfacial polarization [117].

1.2.5 Schottky barrier

The energy barrier for charge carrier exchange between metal- semiconductor is called Schottky barrier (SB) [97]. Charge carriers have to be injected from electronic states in the metal to empty states in the semiconductor and vice versa. Since Si has a band gap and states in the metal are occupied up to the Fermi level, charge carrier transit is not possible for arbitrary energies. The Schottky barrier for electrons Φ_{Bn} (negative) is the excess energy needed for electrons at the Fermi level of the metal to be injected into (empty states of) the semiconductor conduction band. Accordingly, the Schottky barrier for holes Φ_{Bp} (positive) is the excess energy electrons in the metal need to form holes (i.e. empty states), which can be occupied by charge carriers from the valence band of the semiconductor. It follows:

$$\Phi_{\mathrm{Bn}} = \phi_{\mathrm{me}} - (\mathrm{E_C} - \mathrm{E_{vac}}) \tag{1.14}$$

$$\Phi_{\mathrm{Bp}} = \phi_{\mathrm{me}} - (\mathrm{E_V} - \mathrm{E_{vac}}) \tag{1.15}$$

$$\Phi_{\mathrm{Bp}} + \Phi_{\mathrm{Bn}} = \mathrm{E_V} - \mathrm{E_C} = 1.12\mathrm{eV} \tag{1.16}$$

with $\mathrm{E_{vac}}$ vacuum level, $\mathrm{E_C}$ conduction band energy, $\mathrm{E_V}$ valence band energy, ϕ_{me} =work function of the metal. For the interface $NiSi_2$-Si $\Phi_{\mathrm{Bn}} = 0.66\mathrm{eV}$ was reported and consequently $\Phi_{\mathrm{Bp}} = 0.46\mathrm{eV}$ [118]. The SB heights are independent of the doping concentration in the semiconductor. Depending on the work function of the metal ϕ_{me} and doping level, i.e. Fermi level of the semiconductor, charge carriers are exchanged at the interface until the electro chemical potential is in equilibrium. The injected charge in the metal is concentrated at the interface, whereas the charge of opposite sign in the semiconductor is distributed in the space charge region, also called depletion layer with the width $\mathrm{W_D}$. With the charge exchanged, an electric field builds up leading to a built-in potential ϕ_0.

$$\phi_0 = \phi_{\mathrm{me}} - \mathrm{E_F^{Si}} \tag{1.17}$$

The SB heights (values of the energy barrier Φ_{Bn} and Φ_{Bp}) are locally fixed at the metal-semiconductor interface and remain essentially unchanged by electrical voltages across the junction. The reason is that metal screens all electric fields and the whole potential drop occurs solely within the depletion layer (space charge region) in the semiconductor and not across the interface. In contrast to a pn-junction the energy barrier can thus not be levelled completely by applying external bias. However, the effective barrier height is lowered slightly by image-forces [97]. This effective Schottky-barrier lowering effect depends on the voltage across the Schottky junction and also known as Schottky effect. The charge carrier injection is determined by this energy barrier. The energetic situation is shown for electrons in 1.4. By lateral electric fields, i.e. voltage bias ΔV across the Schottky junction, the SB height Φ_{Bn} and thickness (i.e. depletion width) $\mathrm{W_D}$ are modulated[3]

[3]For a SB-FET, ΔV is governed by the source/drain volage $\mathrm{V_{ds}}$ as well as the gate voltage $\mathrm{V_g}$.

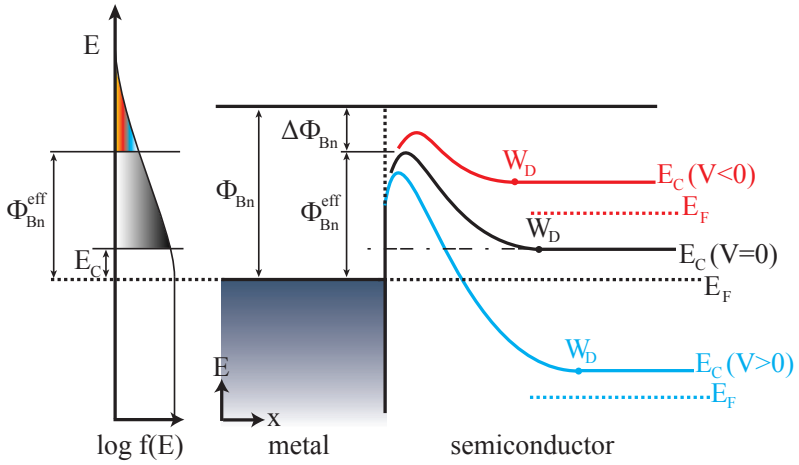

Figure 1.4: Transport through the Schottky junction under bias: (right) energy (E) profile for electrons showing the lower end of the conduction band E_C, (left) Fermi distribution of electrons in metal contact with fraction being able to overcome Schottky-barrier via thermionic emission (color gradient) and fraction being able to tunnel (grey gradient) into energy states of the semiconductor.

depicted in figure 1.4. Charge carriers with energies above $\Phi_{Bn} - \Delta\Phi_{Bn}(\Delta V) = \Phi_{Bn}^{eff}$ can overcome the energy barrier thermally. This injection mechanism is called thermionic emission. The charge carrier energy distribution of metal and semiconductor in thermal equilibrium is determined by the Fermi-Dirac-statistics. The integral over the Fermi distribution f(E) yields the amount of electrons which are able to overcome the energy barrier thermally (with a transmission probability T(E)=1):

$$N_{thermionic} = \int_{\Phi_{Bn}^{eff}}^{\infty} f(E)\,dE. \tag{1.18}$$

For energies below the effective SB Φ_{Bn}^{eff} but above the conduction band energy E_C electrons can tunnel through the barrier. The amount of charge carriers potentially able to tunnel is:

$$N_{tunneling} = \int_{E_C}^{\Phi_{Bn}^{eff}} f(E)\,dE. \tag{1.19}$$

Tunneling is an isoenergetic process. Electrons with energy E in the metal tunnel though the SB in energy states of the same energy in the semiconductor. The transmission probability T(E) for tunneling is non linear[4] dependent on the tunnel barrier thickness $d_n(E)$ at the particular energy E [119]. Therefore, thinning down the Schottky barrier overall by a reduction of the depletion layer width W_D increases the injection rate drastically. The charge carrier injection rate of electrons into the Si channel is proportional to [120, 121]:

$$dN/dt \simeq \int_{\Phi_{E_C}}^{\infty} \bar{T}(E) f(E)\,dE \tag{1.20}$$

[4] exponentially for a rectangular barrier

where $\bar{T}(E)$ is the transmission function which is altered by the Schottky barrier thickness at the respective energy [122]. If E_C is decreased below the metal Fermi level in the biased case, the charge injection increases dramatically since charge carriers are injected from the bulk of the Fermi distribution.

The same consideration can be made for hole injection into the semiconductor [5]. Because of the relation 1.14 decreasing Φ_{Bn} means commonly increasing Φ_{Bp} by selecting ϕ_{me}. For instance, if the metal work function is equal to the semiconductor electron affinity, then $\Phi_{Bn} = 0$eV. The tunnel barrier can be regarded as a serial resistance which depends on the Schottky barrier height and potential bias across the junction. Since Φ_B is commonly not zero for neither holes or electrons for most Schottky contact materials, the tunnel barrier (SB) related serial resistance is a serious drawback of SB-FETs, which limits the output current of the transistor device [123]. $\Delta\Phi_B$ due to the image charge (Schottky) effect is commonly regarded to be small compared to Φ_B. Therefore, the Schottky barrier height Φ_B is regarded further to be fixed at the junction for simplicity. In this case, thermionic emission is limited by the initial Φ_B and can essentially only be turned off under bias ΔV.

1.2.6 SB-FETs

For SB-FETs, source and drain are made out of metal, forming two metal-semiconductor junctions back-to-back. The energy barrier, i.e. Schottky barrier, is naturally resulting from the different energy state distributions of the two materials. As described in the previous section, the values of the Schottky barriers for holes Φ_{Bp} and electrons Φ_{Bn} both depend on the contact metal work function ϕ_{me} only and can not be adjusted by the doping concentration[6]. However, nature does not provide metals with arbitrary ϕ_{me}. To obtain unipolar p-type (n-type) device, a metal with appropriate ϕ_{me} has to be found to maximize Φ_{Bn} (Φ_{Bp}) which minimizes Φ_{Bp} (Φ_{Bn}) at the same time [125]. For complementary logic two metals would have to be implemented which poses a technological difficulty. For most metals, ϕ_{me} yields in both barriers Φ_{Bp} and Φ_{Bn} to be finite. This leads to ambipolar device transfer characteristics, undefined off-state with high off-currents and a SB related serial resistance limiting the on-current. These are reasons why SB-FETs were considered impractical as conventional logic building blocks[7].

Figure 1.5 demonstrates the charge transport in SB-FETs with higher Φ_{Bn} than Φ_{Bp}. Charge carrier injection of holes (p) and electrons (n) on both contacts determines the current through the SB-FET. The band bending profile ($q\Phi_{ch}(x)$), shown in figure 1.5A, depends on the electrical fields throughout the device, which are generated by the applied voltage at source/drain V_{ds} and gate V_g.

[5] For holes, the Schottky barrier height, mobilities and depletion width will be different though

[6] Device doping leads to a prebias and changes the depletion width for one type of charge carrier. For the majority carriers in accumulation mode W_D is reduced. Therefore the SB thickness is lowered and tunneling is highly increased [124]. Nominally undoped devices are used in this work though.

[7] However, it was shown that this issues can be resolved by using a double gate approach leading to reconfigurable electronics [11]

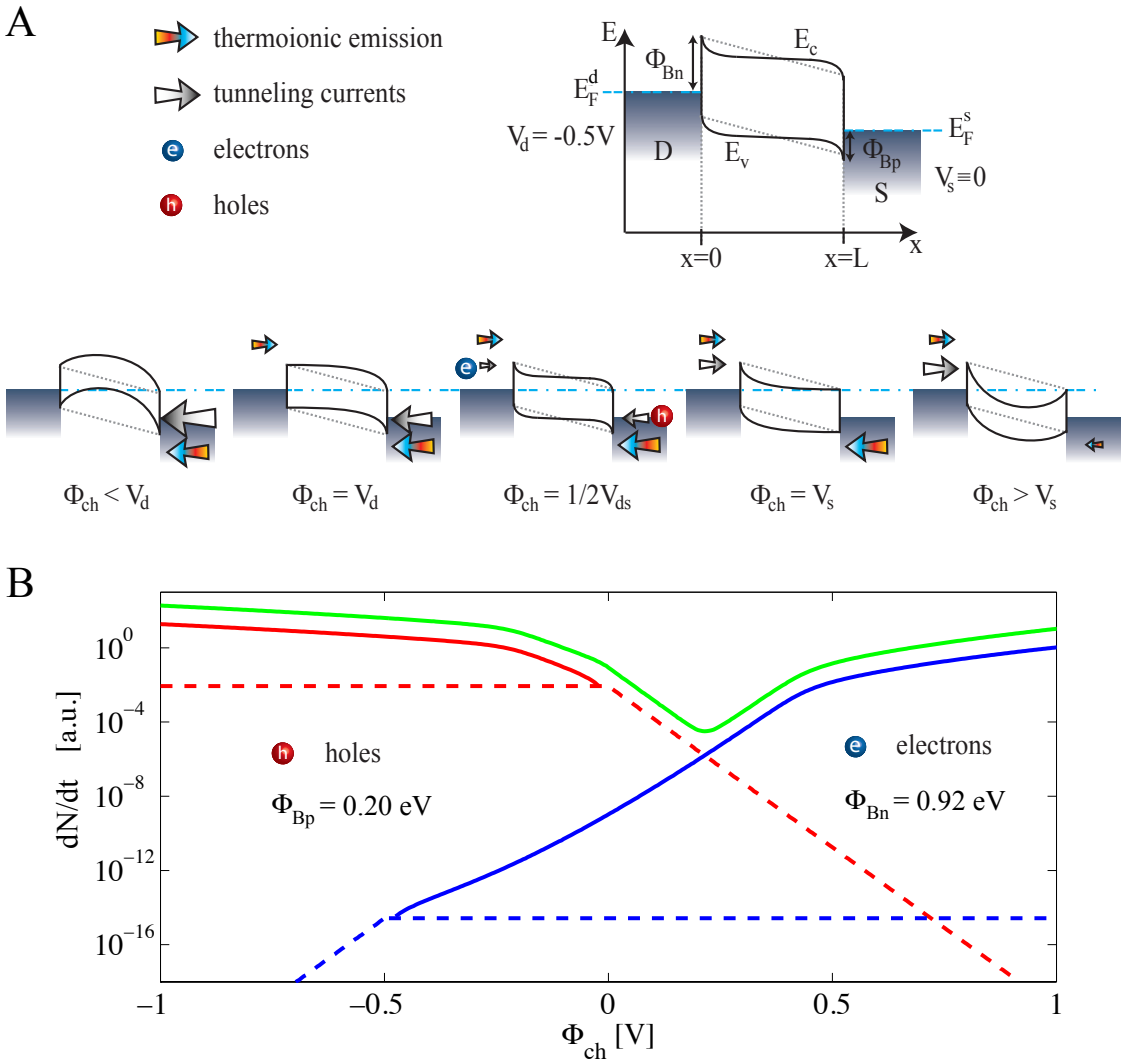

Figure 1.5: Charge transport in Schottky barrier FETs with $\Phi_{Bp} < \Phi_{Bn}$ under bias ($V_{ds} = -0.5V$): A) Band bending profile from source (x=L) to drain (x=0) as a function of channel potential Φ_{ch}. Φ_{ch} is defined as the electric potential at x = L/2. Injection of electrons (dominantly from drain) and holes (dominantly from source) into the semiconductor depends on the band bending at the respective Schottky junction. Electron injection from source and hole injection from drain is neglected here. B) Charge carrier injection rate dN/dt at the junctions for electrons (n) and holes (p) vs. Φ_{ch}. The sum of p- and n-branch (red, blue), represented by the green curve (multiplied by ten for better representation), determines the current through the SB-FET. Two injection mechanisms form the shape of each branch: thermionic emission (dashed line) with a slope of 59 mV/dec (at room temperature) and tunneling (solid line) exhibiting a shallower slope. The maximum thermionic emission rate of p- or n-type carriers is determined by the Schottky barrier height Φ_{Bp} and Φ_{Bn} respectively. For $\Phi_{ch} = V_s$ ($\Phi_{ch} = V_d$), energy bands are flat at the source (drain) contact, tunneling rate of holes (electrons) is zero. From this point, thermionic emission of holes (electrons) is cut off exponentially for $\Phi_{ch} > V_s$ ($\Phi_{ch} < V_d$) and tunneling of holes (electrons) increases for $\Phi_{ch} < V_s$ ($\Phi_{ch} > V_d$). The tunneling probability T(E) depends on the Schottky barrier thickness, which is in turn modified by Φ_{ch}. When the valence (conduction) band drops below the metal Fermi Energy E_F of source (drain), the tunneling rate for holes (electrons) is significantly altered since charge carriers can be injected from highly occupied energy states with $E < E_F$.

For the given V_{ds} of -0.5 V, electrons are predominantly injected from drain and holes from source contact into the channel[8]. The injection rate dN/dt of holes (p) and electrons (n) depends on the position of conduction (E_c) and valence (E_v) band relative to the Fermi level of the contacts and the Schottky barrier thickness (see equation 1.20). Both is controlled by the energy band bending, i.e. the channel potential $\Phi_{ch}(x)$. Injection rate vs. Φ_{ch} is shown in figure 1.5B. Closely linked to this function, is the transfer characteristics by the relations $I_{sd} \sim dN/dt$, $\Phi_{ch} \sim \kappa V_g$. The summation of p- and n-branch (red and blue) results in the observed charge transport dependency on Φ_{ch} (green curve, shifted upwards here for better clearness). At $\Phi_{ch} = 1/2V_{ds}$ bands are bent downwards at the drain and bent upwards at source. Thermionic emission currents (dashed line) of holes (red) and electrons (blue) are limited by Φ_{Bp} and Φ_{Bn} respectively, small tunneling currents (solid line) are enabled. Thermionic emission currents for holes (red dashed) is much larger than for electrons (blue dashed) since $\Phi_{Bp} < \Phi_{Bn}$. By band bending via applied V_g and modification of Φ_{ch}, tunneling currents can be increased for either one of the charge carriers while decreasing tunneling for the other one. Thermionic emission cannot be increased but essentially only turned off[9]. By applying negative V_g, hole currents are increasing, electron currents are decreasing. When $\Phi_{ch} = V_d$, energy bands are locally flattened and tunneling is disabled for electrons. In turn the Schottky barrier thickness at the source junction decreases for holes, p-tunneling increases. If bands are bent further upwards by applying negative V_g, also thermionic emission of electrons is suppressed. The slope of the declining dashed line is 59 mV/dec at room temperature. The Schottky barrier thickness for holes decreases further until a point, when the injection is limited by the (oxide) capacitance of the transistor. Dominantly p-currents are present, the conduction channel will be filled with holes $Q_p \sim (V_g - V_{th})C_{ox}$ and current scales linear with the gate voltage V_g. When going from Φ_{ch} towards positive voltages, hole tunneling stops at $\Phi_{ch} = V_s$, when energy bands are flat at the source junction. However thermionic emission p-currents are still higher than tunneling n-currents. By further bending energy bands down, thermionic emission p-currents continuously decreases and the total current drops until p- and n-branch meet. This intersection point determines position and value of the off-current value which is composed of both p- and n-currents [122].

1.3 ISFET AND BIOFET TECHNOLOGY

ISFET (ion sensitive field effect transistor) technology was first reported 1970 and suggested as device for potentiometric sensing of bio molecules [48, 126–128]. A comprehensive discussion on many aspects of BioFET technology can be found elsewhere [129]. The main motivation for the ISFET was to replace the glass electrode of a pH meter by a transistor. With its high impedance,

[8] Electron injection from source and hole injection from drain is neglected in the following, but has to be considered for a more accurate modelling of charge transport

[9] A small modulating is possible nevertheless, since the effective Schottky depends on the bias

the glass electrode is vulnerable to external noise sources. In contrast, the ISFET enables amplification of the signal directly at the point of the generated half-cell potential, making it resistant to external noise. Then, noise sources limiting the signal to noise ratio come from the ISFET oxide interfaces only. Here, the working principle, analyte concentration dependence of the surface potential and noise sources in Bio- and ISFETs is discussed.

1.3.1 ISFET and BioFET working principle

In ISFET and BioFET technology the gate is replaced by a liquid electrode. The liquid electrode consist of an electrolyte, a weak conductor, containing a reference electrode which controls the electrolyte potential. In contrast to a metal gate, electric fields can penetrate the electrolyte and are screened within the Debye screening length λ_D. Depending on the ionic concentration, i.e charge carrier density ρ, the Debye screening length λ_D in the electrolyte is regulated. Similarly, in the semiconductor, electric fields are screened within the charge carrier density (doping) dependent screening length, also called depletion width W_D, which strongly depends on externally applied electric fields as well. For the case of non present external voltage bias it follows [130]:

$$W_D \simeq \lambda_D \simeq \sqrt{\frac{\epsilon\epsilon_0 k_B T}{\rho e^2}} \tag{1.21}$$

where $\epsilon\epsilon_0$ is the permittivity, $k_B T$ thermal energy, e elementary charge, charge carrier density ρ. Figure 1.6 illustrates the symmetric formation of depletion layers under bias. When voltage is applied between semiconductor substrate and the reference electrode, two depletion layers are formed and charge accumulates from both sides (Si is undoped here). The ISFET can be operated as FET with a polarizable gate. The Si channel conductance changes with the varying potential or charge in the channel. The task of the reference electrode is to convert from electron (metal) to ionic conduction (electrolyte). Conduction in the electrolyte is taking place via ions with low mobility. Electrons do not survive in solutions since they are highly reactive radicals. Commonly used is a reference electrode of second order, i.e. Ag/AgCl [131]. A reference electrode is always needed to stabilize the electrolyte potential by compensating uncontrolled charging by i.e. current leakage through the gate oxide. Depending on the bias $V_{lg} - V_{bulk}$ the device can be operated in the linear or subthreshold regime during measurements.
The oxide surface as well as biomolecules exhibit pH sensitive functional groups (e.g. $-OH$, $-COOH$, $-NH_2$) which are charged depending on pH in solution.

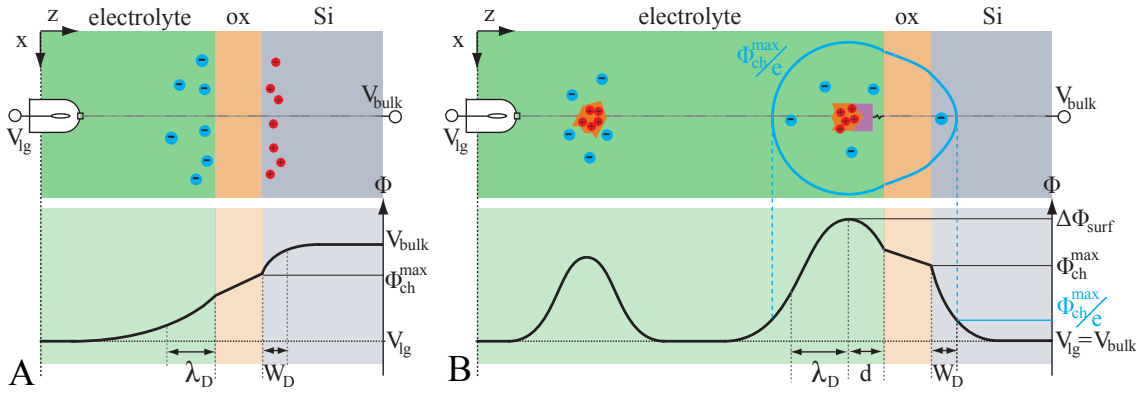

Figure 1.6: Electric potential profiles for sensor devices in electrolytes: A) biased ISFET, for which the metallic gate is replaced with an electrolyte gate. Depletion layer are formed at both sides [132]. B) BioFET sensor. Molecule exhibit charged groups which are compensated by counter ions in solution. When molecules bind to the sensor surface, the inherent charge is screened from the electrolyte and semiconductor side. Depending on the transistor working regime, charge is accumulated in the Si conduction channel and the channel potential Φ_{ch} is modified. Blue sphere shows the equipotential line for which Φ_{ch} has decayed by a factor of $1/e$ in the subthreshold regime.

Those groups are amphoteric (A), i.e. they are able to donate ($-COO^-$, $-NH^-$, $-O^-$) or accept ($-COOH_2^+$, $-NH_3^+$, $-OH^+$) a proton by the reactions:

$$AH \rightleftharpoons A^- + H^+ \tag{1.22}$$

$$AH + H^+ \rightleftharpoons AH^{2+} \tag{1.23}$$

The Gibbs free energy[10] G(p,T) determines the thermodynamical equilibrium for biochemical reactions in solutions, here exemplarily for deprotonation:

$$\Delta G = G_{products} - G_{educts} \tag{1.24}$$

$$G_{educts} = \left(G^0_{AH} + k_B T \cdot \ln(c_{AH})\right) \tag{1.25}$$

$$G_{products} = \left(G^0_{H^+} + k_B T \cdot \ln(c_{H^+})\right) + \left(G^0_{A^-} + k_B T \cdot \ln(c_{A^-})\right) \tag{1.26}$$

$$\Delta G = \Delta G^0 + k_B T \cdot \ln\left(\frac{c_{H^+} c_{A^-}}{c_{AH}}\right) \tag{1.27}$$

where c(i) are the concentrations of deprotonized and neutral groups. ΔG^0 is the change of Gibbs free enthalpy when the reaction 1.22 runs from left to right side. $\Delta G^0 = \Delta H^0 - T\Delta S^0$ is composed of the change in enthalphy[11] ΔH^0 and the change in entropy ΔS^0 for each single reaction. The right term in 1.27 represents the endeavor to maximize the entropy of the system by regulating the concentrations. So even if ΔG^0 is positive, the reaction 1.22 will run to increase $c_{H^+}c_{A^-}$ at the expense of c_{AH} until $\Delta G = 0$, because thereby the total entropy of the system increases. At

[10] Since in solution pressure p and temperature T remain constant during biochemical reactions the system is unambiguously characterized by G(p,T).

[11] which is associated with the bond-dissociation energy

equilibrium $\Delta G = 0$, when the total entropy is maximized, the product of concentrations is a reaction constant K_a:

$$\Delta G^0 = -k_B T \cdot \ln(K_a) \tag{1.28}$$

$$K_a = \frac{c_{H^+} c_{A^-}}{c_{AH}} \tag{1.29}$$

$$pK_a = -\log(K_a) \tag{1.30}$$

$$pK_a - pH = -\log\left(\frac{c_{A^-}}{c_{AH}}\right) \tag{1.31}$$

where pK_a is the equilibrium constant, describing the degree of deprotonation in thermal equilibrium depending on pH. The same considerations are valid for any chemical reaction, e.g. the basic reaction with equilibrium constant pK_b and the analyte-receptor reaction. The pH value for amphoteric functional groups being charge neutral is called isoelectric point or point of zero charge pK_Z and is related to the pK_a and pK_b values. The pK_a and pK_b values describe the strength of the acid and base component of the amphoteric group. Charged groups (A^-, AH_2^+) are surrounded by counter ions in solution (e.g. Cl^-, H^+), the complex as such is charge neutral. However, electric fields are locally generated around the localized deprotonized donor A^- due to the charge separation forming a multipole. The Gibbs relations given above are only valid if the reaction is never affected by electric fields, i.e. when the functional groups AH are spatially separated more than the extensions of the formed multipole. However, this is not the case for a pH sensitive oxide, where the binding sites (AH) are chemically localized in close vicinity with surface densities of ~ 5 AH nm^{-2} [133]. If many charged groups A^- are present already on the oxide in close vicinity, their electric fields add up changing the electrical potential between electrolyte and surface $\Delta\Phi_{surf}$. For this case, the site binding model describes the pH ($-\log(c_{H^+})$) dependence of the surface potential Φ_{surf} [127, 134]. To (de)protonate an adjacent AH group, the corresponding H^+ has to do additional electrical work $-q\Delta\Phi_{surf}$ when the reaction 1.22 should occur. This leads to an additional energy term $-q\Delta\Phi_{surf}$ in the Gibbs relation, shifting the equilibrium for both basic and acidic reactions.

$$\Delta G_{acid} = \Delta G^0_{acid} + k_B T \cdot \ln\left(\frac{c_{H^+} c_{A^-}}{c_{AH}}\right) - q\Delta\Phi_{surf} \tag{1.32}$$

$$\Delta G_{basic} = \Delta G^0_{basic} + k_B T \cdot \ln\left(\frac{c_{AH^{2+}}}{c_{H^+} c_{AH}}\right) - q\Delta\Phi_{surf} \tag{1.33}$$

$$\sigma_{surf} = e \cdot c_{AH_2^+} - e \cdot c_{A^-} \tag{1.34}$$

$$\Delta\Phi_{surf} = \Delta\sigma_{surf}/(C_{ISFET} + C_{DL}) \tag{1.35}$$

The reactions 1.22 and 1.23 run until limited by ΔG^0 or $q\Delta\Phi_{surf}$. The surface potential Φ_{surf} is coupled to the surface charge density σ_{surf} and capacitances of ISFET and double layer [134]. When c_{AH} is large, i.e. there are many amphoteric groups close together, only a small fraction of the AH-groups has to be ionized to increase Φ_{surf}. The reaction will then essentially be limited by

$q\Delta\Phi_{surf}$, i.e. the generated electric fields. In this case Φ_{surf} is changing with pH according to the Nernst limit, which is given by natural constants and the temperature:

$$\Delta\Phi_{surf} = \frac{kT}{e}\ln(10) \cdot \log(c_{H^+}/c^0_{H^+}) = 59mV/dec \cdot \log(c_{H^+}/c^0_{H^+}) = 59mV/pH \cdot \Delta pH \qquad (1.36)$$

Interestingly, 59 mV/dec is the same slope like already found for the transistor subthreshold regime. The reason is, that in both cases diffusion of charges species (entropy) is compensated and limited by built-up electric fields. Indeed, the surface charge density σ_{surf} will adapt accordingly to the capacitances $C_{ISFET} + C_{DL}$ and the surface potential Φ_{surf}, which is determined by the pH value. However, if ΔG^0 or c_{AH} are very small, the reactions 1.22 and 1.23 cannot yield in enough σ_{surf} to built-up Φ_{surf}. This also occurs when the ionized groups are spatially separated too much and their charge is screened by counter ions. The reactions are then intrinsically inhibited and pH response $\partial\Phi_{surf}/\partial pH$ is smaller than 59 mV/pH. The site binding model can explain the pH sensitivity of ISFETs for various gate oxide layers depending on the well-known pK_a and pK_b values of their amphoteric groups, which are normally used instead of ΔG^0. For SiO_2 with c_{AH} of $5 \cdot 10^{14} cm^{-2}$, pK_a -2, pK_b 6, the surface buffers strongly at the point of zero charge pK_Z 2-2.5 [67, 135]. Naturally, only few amphoteric groups (silanol) are ionized, electric fields are not built-up and pH response is consequently significantly reduced around pK_Z. For Al_2O_3 with c_{AH} of $8 \cdot 10^{14}$, pK_a 6, pK_b 10, where pK_a-pK_b is small, protonation and deprotonation are not inherently inhibited [67, 135]. An almost Nerstian response of 55 mV/dec was found for Al_2O_3 for large ranges of pH values, although $\partial\Phi_{surf}/\partial pH$ decreases little at $(pK_a+pK_b)/2 \sim pK_Z$ [127]. Other ion sensitive oxides like Si_3N_4, silicon oxynitride and Ta_2O_5 were proposed as well for pH sensor applications [136–138].

For ISFETs, $\Delta\Phi_{surf}$ can be regarded as an additional built-in potential created by chemical surface reactions. It is proportional to the logarithm of the analyte (H^+) concentration because of the equations 1.32 and adds up to the flatband voltage V_{FB} and threshold voltage V_{th} [128]:

$$V_{FB} = V^0_{FB} + \Delta\Phi_{surf} \qquad (1.37)$$

$$V_{th} = V^0_{th} + \Delta\Phi_{surf} \qquad (1.38)$$

When not limited by c_{AH}, the surface charge density σ_{surf} adapts accordingly to $C_{ISFET} + C_{DL}$ [132]. The modified V_{FB} or V_{th} leads to a shift of the transfer characteristics by $\Delta\Phi_{surf}$ which can be measured in constant voltage (V_{lg}, V_{bulk} = const.) or constant current (I_{sd} = const.) mode. In constant voltage mode, I_{sd} over time and the transient change in surface potential is derived over the transconductance $\partial I_{sd}/\partial V_{lg}$:

$$\Delta\Phi_{surf} = \Delta I_{sd}\frac{\partial V_{lg}}{\partial I_{sd}} \qquad (1.39)$$

Since the transconductance is a function of the surface potential itself, the analysis in not straight

forward. In constant current mode, V_{lg} is regulated over a feedback loop to keep $\Phi_{surf} = V_{lg} + \Delta\Phi_{surf}$ and thus I_{sd} constant [128]. $\Delta V_{lg} = -\Delta\Phi_{surf}$ can directly be read out without the need to consider the transconductance at all. However, also for constant current mode higher transconductance will lead a more accurate feedback and measurement.

The site binding model does not consider inhomogeneities in the surface potential for low concentrations of charged surface groups which will limit its use for biosensor modelling. For a BioFET, receptor molecules are chemically bound to the oxide surface. Receptor molecules can be proteins or aptamers (short single strands of DNA) which bind specific target molecules reversibly. Binding is non covalent but by hydrophobic/hydrophilic and electrostatic interactions like hydrogen, ionic and Van-der-Waals bonding [139, 140]. Associated with the complex formation of target molecule and receptor is the binding enthalpy ΔH^0. The charged pH sensitive functional groups (e.g. COO^-, NH_3^+) of biomolecules are screened by counter ions in solution (e.g. Cl^-, H^+) [141]. The complex of molecule and ionic cloud is charge neutral but exhibits a multipole moment. When the molecule binds to the surface, the oxide layer poses a steric hindrance for ions. The charge on the molecule is screened partly by charge in the electrolyte and semiconductor and from the polarization of the oxide [132]. The multipole moment, i.e. potential distribution in this situation, changes which is associated with a certain increase of electrical potential energy ΔE_{el} and probably entropy which can be incorporated in the Gibbs free energy term ΔG^0. Figure 1.6 shows the electrical potential around the analyte-receptor complex. From its maximum value $\Delta\Phi_{surf}$, the screened potential is dropping in the electrolyte towards the oxide interface. To increase the sensitivity by a large modulation of the potential inside the Si channel, the receptor should be located as close as possible to the surface by minimizing the chemical linker length (d). The charged complex affects the surface potential around it within a radius of the Debye length λ_D. In figure 1.6 this is illustrated as volume inside the blue line. If the analyte concentration on the surface is high and analyte targets bind within a distance smaller than $2\lambda_D$ of each other, they have to do work in the electrical field of attached complexes which lead to a term $\Delta\Phi_{surf}$ similar to equation 1.32. If the concentration is low and analyte targets are not interacting electrostatically, since their spacial separation is much larger than $2\lambda_D$, this term vanishes. This scenario might be realistic for point of care diagnostics with targeted extreme low volumes ($\sim \mu$l), concentrations ($\sim$ fM) and consequently analyte targets (few hundred). The generated potential inside the BioFET is then only determined by energy terms of the deformed electric multipole in ΔG^0 and independent of the analyte concentration.

1.3.2 Noise in ISFETs

Noise is determining the lower detection limit of the sensor. The intrinsic noise of the sensor element and the fluctuating surface potential at the electrolyte-oxide interface generate noise in

the first place [64, 66, 74]. Transistor noise is related to statistic tunneling through SB (shot noise), charge scattering and trapping as well as generation/recombination (G/R) noise in the conduction channel and polarization noise of the dielectric. Additional noise is produced in the serial resistivities, e.g. the thin inter electrodes. Since only slow processes and long term changes in the surface potential are to be measured in biosensors, high frequency noise components can be filtered with a low pass or averaging over time. The low frequency transistor noise is discussed to be generated by mobility ($\Delta\mu$) and/or number fluctuations (ΔN)[142, 143]. Mobility fluctuations are caused by statistical scattering of charge carriers at defects (e.g. dopants) reducing their mobility. Number fluctuations are caused by random trapping and release of charge carriers at interface traps leading to variations of the charge carrier number in the conduction channel. However, both mechanisms lead to a frequency dependent (current) noise power spectral density S_I described by [144]:

$$S_I = \frac{I_{sd}^2 * \alpha}{f^{\beta} N} \tag{1.40}$$

where N is the amount of charge carriers in the conduction channel Q_{ch}/e, β the exponent of the 1/f frequency dependence and α is a constant describing the noise predisposition. This equation can be employed to describe both noise mechanisms qualitatively, since the only assumption behind is, that whatever electrons do to cause noise, they do it independently [142]. Using a low pass with cutoff frequency F to filter the high frequency noise component (e.g. f>1Hz) the signal to noise ratio (SNR) can be improved. The rms (root mean square) value σ_I of I_{sd} is then given by an integral of all noise components with distinct frequencies up to F:

$$\sigma_I = \sqrt{\int_0^F S_I(f)\,df} \sim I_{sd}\sqrt{\frac{\alpha}{1Hz^{\beta} N}} \tag{1.41}$$

So the current noise σ_I is proportional to the current I_{sd}. Because contributions of individual charge carriers to the total noise are uncorrelated, σ_I is inversly proportional to the square root of N, the amount of charge carriers.

$$SNR = \frac{\Delta I_{sd}}{\sigma_I} = \frac{\Delta V_{th}}{\sigma_I}\frac{\partial I_{sd}}{\partial V_g}. \tag{1.42}$$

The SNR is thus proportional to the transconductance to current noise ratio [63]. We can also see with equation 3.4 that the SNR increases with the square root of the charge carrier amount $\sqrt{N}$. Noise is also generated at the electrolyte/oxide interface. The brownian motion of charged ions leads to a fluctuation surface potential. This noise source is inversly proportional to the charge carrier concentration, i.e. ionic strength [65, 66]. For biosensors it was observed that fast reaction kinetics of anaylte binding and detachment (i.e. exchange current density) at the surface leads to additional noise components with a non 1/f frequency behaviour [145]. Slow binding kinetics do not manifest as noise but can be electrically resolved and quantified [146].

2 FABRICATION OF SCHOTTKY BARRIER FET PARALLEL ARRAYS

In this section the technology of the fabrication process for SB-FET parallel arrays is summarized. Also the initial process for producing single nanowire devices will be discussed and explained how this process had to be changed in order to obtain devices which can be employed for biosensing. Process details are given after an overview of the process flow.

2.1 STARTING POINT OF DEVICE FABRICATION

In the initial stage of nanowire SB-FET production only single nanowire devices could be produced from bottom-up grown nanowires and was already described in [77–79]. Temperature and plasma assited coalescence of a sputtered Au layer was employed to produce Au particles for growth (growth is described in section 2.2.2). This method leads to large variations of the Au seed particles which is reflected in the nanowire diameter distribution. Nanowires were detached from the growth substrate by sonication in isopropanol, a solvent in which they are dissolved without forming aggregates. The nanowire solution is sprayed on Si/SiO_2 (degenerately p-doped/20 nm oxide) chips with pre patterned Ti/Co (10 nm/20 nm) electrodes. A non uniform coverage with randomly orientated nanowires and low density is the result. Nevertheless this approach prevents nanowire agglomeration which enables contacting of single nanowires. Occasionally, a single nanowire happens to lay across two of the pre patterned Ti/Co electrodes at the same time. Since the nanowire placement is unguided, the probability for this coincidentally situation is low and thus the device production yield is less than 5%. The nanowires were embedded in 40-80 nm Ni, which is deposited

on top of the Ti/Co contacts via electroless plating [78] [1]. To form a good electrical contact and abrupt $NiSi_2$-Si interfaces, the chip is annealed in 450 °C forming gas (H_2/N_2, 1/20 p/p). Prior to the anneal the chip is dipped into 1% NH_4F buffered HF to etch back the SiO_2 oxide shell of the nanowire which would otherwise prevent the Ni inter diffusion. For this reason the single nanowire devices always had a native oxide shell grown at room temperature, which exhibits a lot of charge trapping sites [147, 148]. Annealing at temperatures above 450 °C leads to the formation of the $NiSi_2$ nickel disilicide phase, which obtains a higher resistivity than NiSi but is known to form very sharp interfaces to Si. Rough interfaces have to be avoided especially SB-FET devices since they lead to random variations of the effective Schottky barrier, therefore the byproduct of increased serial resistance is accepted.

2.2 PARALLEL ARRAY TRANSISTOR AND SENSOR DEVICES

The fabrication procedure, like described in the previous section, could not have been easily modified to generate parallel array devices suitable for sensor applications and capable of being operated in electrolytes. For this reason the fabrication procedure was fundamentally modified. The key points of the process flow for nanowire parallel array fabrication are visualized in figure 2.1. An explanation on the necessity and details on the processes is given in the attached subchapters.

1. Au nanoparticle (GNP) deposition on growth substrate by dip coating in GNP solution
2. incineration of organic residues by O_2 plasma and oxygen anneal
3. CVD growth of 40 μm long Si nanowires
4. contact printing transfer of grown nanowires to the chip substrate (Si/SiO_2 stack) forming parallel arrays
5. removal of AuSi eutectic tips of the nanowires by immersion in HCl/HNO_3 etchant
6. partial dry oxidation of the nanowires to form low defect oxide shell
7. UV-lithographic definition of electrode patterns on top of nanowire layer
8. nanowire oxide shell removal locally under the electrodes by HF etching and Ni deposition
9. thermally driven incomplete silicidation of nanowires forming $NiSi_2$-Si interfaces
10. Al_2O_3 atomic layer deposition on the entire chip surface and UV-lithographic patterning for local Al_2O_3 removal over electrical contact pads

This is the basic procedure to produce SB-FET which can be operated in electrolytes. Optionally, further layers can be deposited for on chip quasi reference electrodes (1), top gates (2) or Schottky junction passivation (3).

[1] For electroless plating, the chip is immersed in aqueous solution containing Ni salt at a temperature of 85 °C. The Ni salt is reduced at the catalytically active Co and later on self catalytically active Ni, leaving the Ni layer on top.

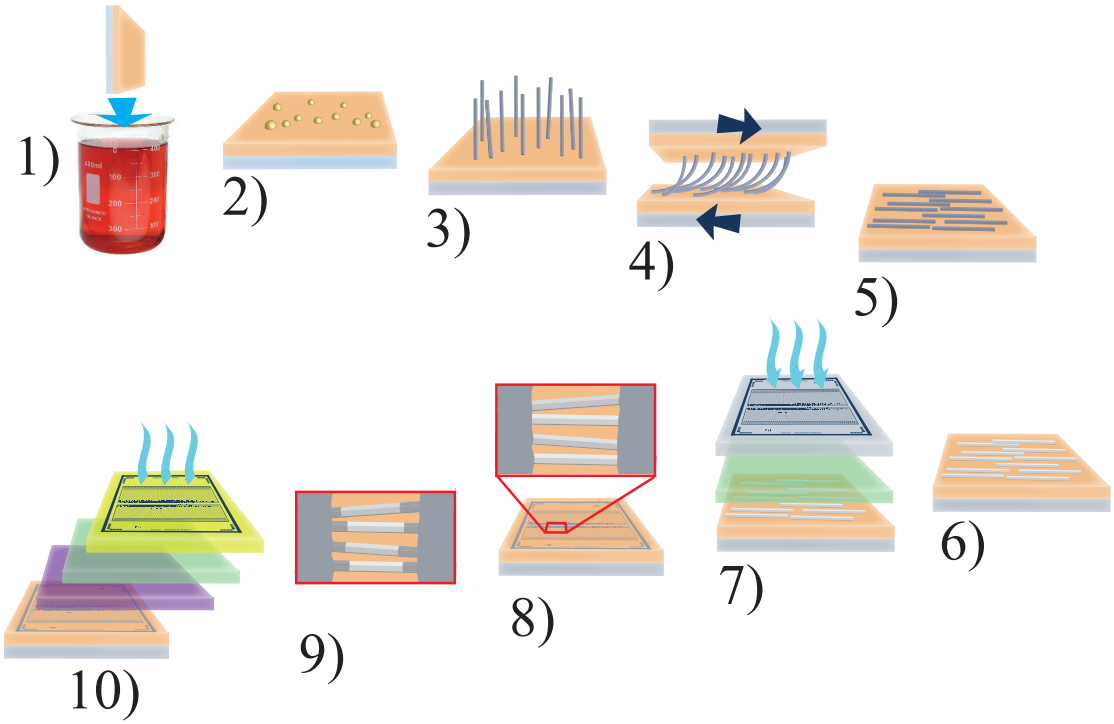

Figure 2.1: Process flow of parallel nanowire SB-FET fabrication: all process steps to the basic platform. Description is found in the main text.

1. UV-lithographic patterning of Ag electrodes is done on top of the Al_2O_3. By chlorination of the Ag, forming AgCl on the surface, a quasi reference electrode is obtained.
2. Meander shaped or all-over planar top gates are patterend by UV-lithography, Ni/Pt (20 nm/10 nm) sputtering and liftoff
3. For SB-passivation, a SU8 photo resist masking layer is patterned by UV-lithography. The SU8 layer is hardened by a postbake and covered completely with Al_2O_3 by ALD. Al_2O_3 is back etched at the contact pads as described before.

2.2.1 Gold nano particle deposition

Since gold layer coalescence is forming irregular Au particle sizes, synthesized gold nanoparticles (GNPs, Plano GmbH) were used as seed particles. To prevent gold particle aggregation on the substrate and assure high seed particle densities, a poly(diallyldimethylammonium chloride) (PDDA, Sigma Aldrich) monolayer is firstly deposited [149]. Si growth wafers (up to 8 inch, p-doped boron $1^{16}cm^3$) with native oxide surface are cleaned with acetone, isopropanol and surface activated by O_2 plasma. They are immersed in 1 mM PDDA in DI water for 2 min and afterwards rinsed under a stream of DI water. Subsequently, the substrates are immersed in the GNP solution for 1 min, leading to a homogeneous seed particle distribution without agglomerations [150]. The wafer is

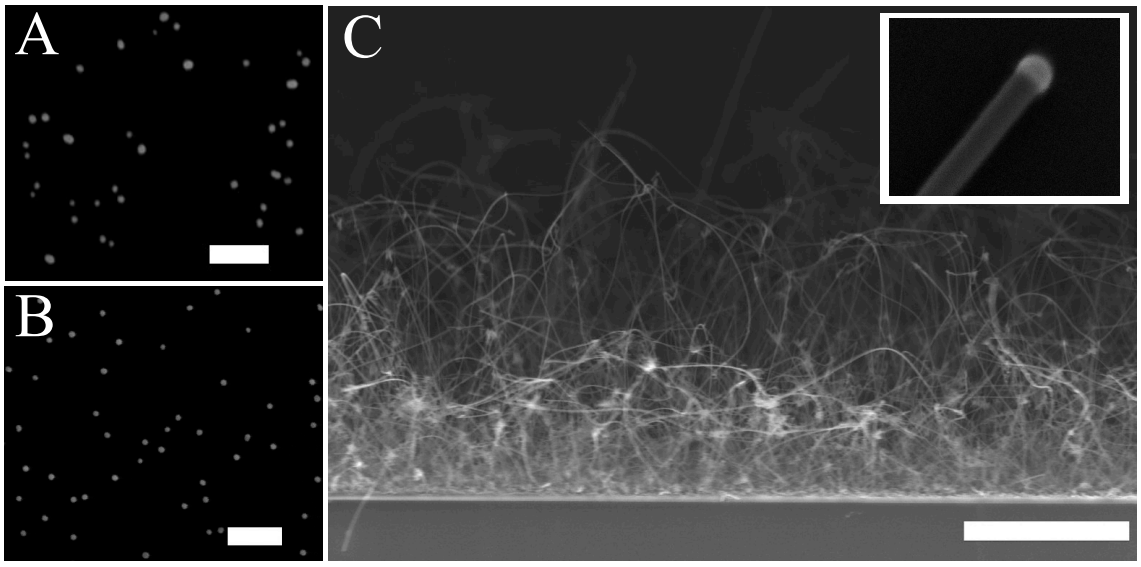

Figure 2.2: SEM images of growth substrate before and after growth: A) Au seed particles produced by coalescence of 0.5nm thick sputtered Au layer (scale bar 200nm). High size non-uniformity is evident. B) Synthesized Au seed particles deposited via dip coating (scale bar 200nm). Size uniformity increased. C) SEM side view of bottom-up grown Si nanowires (scale bar 10μm). Amorphous Si is precipitated at the substrate bottom. At a distance from the substrate surface nanowires are well separated and no amorphous Si is found. Inset depicts nanowire tip with AuSi eutectic droplet remaining on top after growth.

rinsed with DI water for 4 min to remove ions originating from the GNP solution. The GNP citrate shell exhibits a negative charge in solution at pH 7, whereas the PDDA side chain exhibits a positive charge. Therefore the GNPs are strongly adhering to the substrate and are not removed from the surface by water cleaning. The surface coverage with GNPs is highly uniform, the density can be adjusted by the immersion time. Organic residues are removed by incineration in O_2 plasma (10 mbar, flow rate 200 sccm, temperature 400 °C) for 15 min followed by anneal in O_2 atmosphere (125 mbar, flow rate 200 sccm, temperature 400 °C) to avoid contaminants during the subsequent nanowire growth. Cleaned growth substrates were transferred into a CVD hot-wall reactor for nanowire growth.

2.2.2 Bottom-up growth of Si nanowires

In this work a hot wall reactor CVD furnace (ATV Technologie GmbH) was employed for bottom-up nanowire growth. Silane SiH_4 was used as precursor. Si growth wafers (up to 8 inch, p-doped boron $10^{16}cm^3$) coated with Au particles are introduced in the CVD hot-wall reactor. The CVD furnace is heated to 450 °C in H_2 atmosphere at a pressure of 65 mbar [77]. After reaching the temperature plateau of 450 °C and a stabilization time of 5 min, SiH_4 is introduced. A partial pressure ratio H_2/SiH_4 of 10/1 p/p is adjusted by the flow rates of individual mass flow control units for each gas. The pressure is kept stable via an automatic pressure sensor controlled

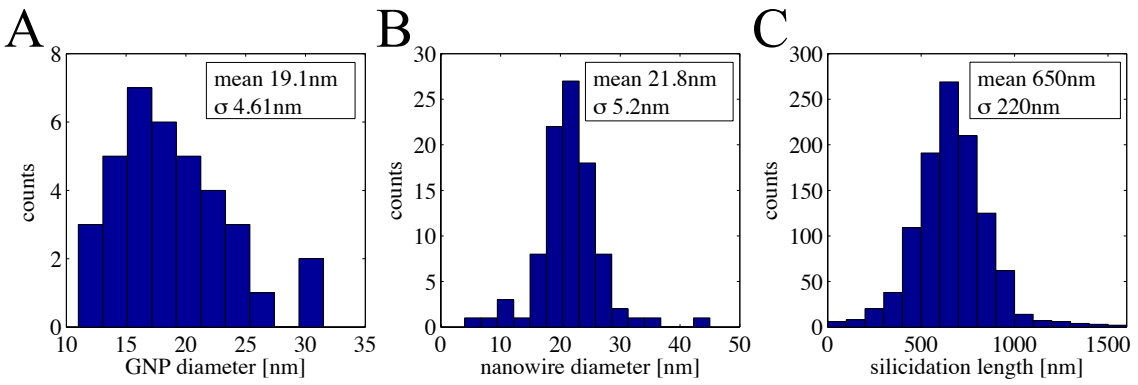

Figure 2.3: Histograms showing statistical variations in nanowire ensemble during fabrication: A) GNP seed particle size distribution, GNP diameters were extracted from TEM measurements. B) Resulting nanowire diameter after growth with GNP seed particles. Diameters were extracted from AFM measurements of contact printed aligned nanowires. Resulting nanowire arrays with native nanowire oxide shell were contacted to Ni electrodes and Ni-silicidized for 30 sec. C) Silicidation length of individual nanowires in the array. The resulting length distribution of silicidized nanowire segments might be affected by the nanowire diameter, i.e. volume distribution.

feedback loop. The resulting nanowire length is proportional to the exposure duration to the H_2/SiH_4 composite. Commonly the duration was chosen as 40 min and lead to approx. 40 μm long nanowires estimated from SEM side pictures shown in figure 2.2. Amorphous Si is deposited around the nanowire base close to the substrate surface as well. Nevertheless, further away from the substrate, amorphous Si is not found and the nanowires show a uniform diameter along the whole nanowire length. TEM investigations show a monocrystalline structure of the Si nanowire and an amorphous SiO_2 shell [151]. A study of Au particle and nanowire size is depicted in figure 2.3. Au clusters were investigated via TEM (Zeiss Libra 200 MC), acquisition of the diameter statistics was done manually. Nanowire diameter statistics were obtained by analyzing the topography of AFM (Digital Instruments, Multimode AFM 2) pictures taken in tapping mode. For simplification, the nanowire cross section was approximated to be round. Since the actual lateral extensions of the nanowire are broadened by tip effects on the topography map, the maximal heights were used as values for the diameter. The mean diameter values of the Au particles d_{Au} (19.1 nm) and the nanowires d_{NW} (21.9 nm) are correlated, the ratio is 1.14. This is in agreement with the eutectic diagram predictions of 20% fractional Si in the AuSi droplet which leads to a diameter increase compared to the initial Au droplet resulting in $d_{NW} > d_{Au}$ (see section 1.1). The diameter standard deviations of approx. 5 nm are comparable. This implies that initial variations in the Au particles determine the nanowire diameter distribution which shows the importance for uniform seed particle sizes. Although the impact of volume Ni diffusion is regarded to be neglectable from many groups, the nanowire diameter and thus volume may affect the silicidation length. The histogram of silicidation lengths in a nanowire parallel array is depicted in figure 2.3 and is discussed in detail in section 2.2.8.

2.2.3 Nanowire deposition methods

There are plenty of deposition methods described for bottom-up grown Si nanowires in the literature including flow alignment, dielectrophoresis, Langmuir-Blodgett assembly and contact printing [23–25, 152, 153]. Most techniques rely on the basis of manipulating nanowires in suspensions. Hence, a dewetting of the nanowires is necessary which often leads to complications. During this work 3 different alignment techniques were tested.

Langmuir-Blodgett

Langmuir-Blodgett machines are commonly used to densify monolayers of molecules floating on a water surface and transfer them on an arbitrary substrate as an easy tool to arrange molecular electronics [154, 155]. This technique uses the fact, that monolayers of amphiphilic molecules are easily formed on water surfaces. The machine involves a Teflon trough filled with water to the top and two Teflon barriers in contact with the water surface. A hydrophobic substrate is partly dipped into the water with its surface normal perpendicular to the water surface. The Teflon barriers are running on the trough's boundaries towards each other to compress the floating molecules between them. The surface tension is surveilled with a so called Wilhelmy-plate dipped into the water, connected to a spring balance. When the layer is sufficiently densified, the substrate is drawn out of the water with constant velocity while the barrier positions are regulated with a feedback loop to maintain the chosen surface tension for transfer. With the hydrophilic SiO_2 shell Si nanowires would just sink and be dissolved in water. Therefore, they have to be hydrophobizied firstly to make them float on the water surface. Si nanowires are mixed with a tensile named octadecylamine in isopropanol solution to render them hydrophobic. The hydrophilic heads of octadecylamine are reversibly bound (Van der Waals interactions) to the nanowire while the hydrophbic tails are pointing outwards. The solution is then spread on the water surface. The recipe is imitated from [152]. Densification and transfer happened like described above. Although dense layers can be achieved, the obtained films do not show a preferred orientation. Nanowires are overlapping and multiple Si grains and remnants from solution can be observed. The remnants, particles and contaminants are also observed for spray coated nanowire films. It is assumed that grains and particles are formed during sonication. Sonication is likely to detach the amorphous Si materials and malformed nanowires from the growth substrate bottom as well. Such contaminants are mixed into the solutions as well and cannot be selectively filtered. Since thin and long nanowires are very flexible, they tend to bend and curl up during the film densification. This is regarded as a general problem of LB. Particles and contaminants are regarded as common issue of nanowire solution generation.

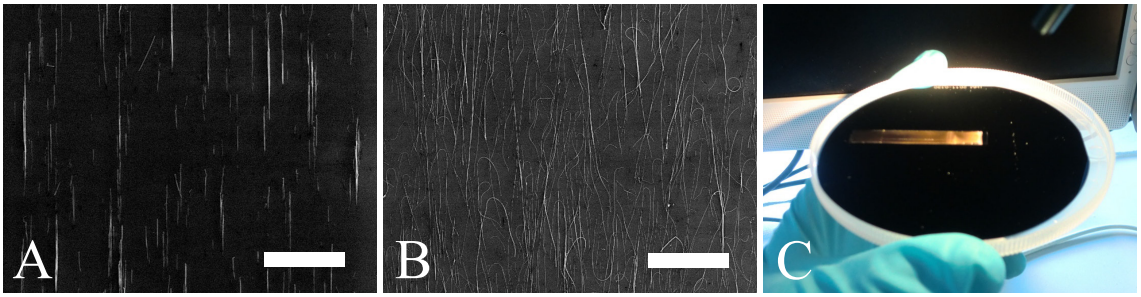

Figure 2.4: Illustration of contact printed nanowire arrays: SEM images of A) short and B) long nanowires (diameter 20nm) after printing transfer (scale bar 5μm). Short nanowires show perfect alignment but are difficult to contact electrically. Long nanowires curl up occasionally but show acceptable alignment and high density. C) 4 inch wafer with 400nm thermally grown front oxide and contact printed nanowire parallel arrays. Interference colors reveal the nanowire layer.

Adhesion tape transfer

As an option for a direct transfer of nanowires from the growth substrate to the chip substrate, a glue tape transfer was considered since even Nobel Prizes can be won with such trivial techniques [156]. Tesa tape was sticked to the growth substrate surface and detached with an optical evidently seen yellow layer of nanowires. The glue tape is attached to a donor substrate and subsequently dissolved in acetone. Ultra dense layers of nanowires can be transferred in this way. Unfortunately they are not orientated, multilayered and a very high concentration of unknown sort of contaminant was observed, which cannot be removed by incineration or oxygen anneals. So this techniques was rated completely inappropriate.

Contact printing/ smearing transfer

The method of choice for parallel arrays of nanowire transistors in this work was contact printing, or smearing transfer as people call it [152, 157, 158]. No lubricant or chemical surface treatments, like suggested by other authors, were employed to reduce contamination risk further. The growth sample with vertically grown nanowires is divided into smaller pieces, called donor substrates, with dimensions of 12 mm x 12 mm x 0.625 mm. A steel cubic weight with edge length 11 mm is attached to the donor substrate's back with double sided glue tape. The donor substrate is cleaned with N_2 pistol to remove dust and silicon grains and placed up side down on a receiver chip substrate (Si/SiO_2, degenerately p-doped/400 nm, cleaned with water/acetone/isopropanol/N_2 purge) with dimensions 25 mm x 25 mm. The metal weight ensures a defined pressure between the substrates. The donor is moved by pushing the side of the wafer piece with tweezers for several millimeters until the friction forces are increasing drastically at an indefinable point. Strong forces have to be applied pushing the side of the donor substrate until static friction is replaced by dynamic friction again. Nanowires are ripped off the donor substrate at that point, optically noticeable by

interference colors on the receiver substrate. Nanowires are being oriented during the sliding in direction of movement and stick to the receiver substrate probably even by covalent bonding. Fusion of Si-hydroxyl groups (SiOH) forming covalent Si-O-Si bond under water formation is commonly known to exist [159]. In presence of water at SiO_2 surfaces hydroxyl groups are always present. Although other groups assumed Van der Waals interaction based forces between nanowires and receiver substrate, a covalent binding seems more convincing since adhesion is extremely strong. Nanowires do not detach from substrate when the chip is immersed in arbitrary solvents, not even during sonication. The drastic building up of friction forces is assumed to arise from release of an air cushion between the substrates. As soon as nanowire are laying lengthways touching the receiver substrate, a large surface area of the nanowire is in contact with the receiver substrate. Resulting adhesion forces are thus strong enough to rupture bonds at the nanowire bottom to detach it from the donor substrate. Macroscopic forces are built-up when many nanowires are starting to attach to the substrate and the net contact area is large. Then the substrates stick strongly together and can hardly be moved.
Depending on the Si oxide layer on the donor substrate, contact printed nanowire layers are perfectly visible in the optical microscope, even individual nanowires can be identified. Highly orientated and dense layers can be achieved with this technique. Most important, the nanowire surface has not to be modified for the transfer. Lower parts of the nanowires and amorphous material from the bottom of the growth substrate are not transferred during the process. This leads to a very clean layer without obvious contaminations. However, the SiO_2 layer on the donor substrate is easily damaged by present dust grains and Si particles during the printing process. A rupture of the later gate dielectric leads to gate leakage and inoperable devices. Therefore, such contaminants have to be carefully removed from the substrates prior to printing and a thick SiO_2 back gate oxide is preferred.

2.2.4 Nanowire oxidation

The need for a thermally grown silicon oxide (SiO_2) on Si nanowires arises from the requirement of low charge trapping and noise. Native SiO_2 has a poor electrical performance and is hygroscopic [147, 148, 160]. However, thermally grown Si/SiO_2 interfaces have very low surface state densities [161]. Surface Fermi level pinning and trapping due to mid gap located energy states is minimized [162]. In fact, the reason for silicon being used for electronics in the last decades is mainly for its good quality (low trap density), easy to produce and chemically stable own oxide SiO_2.
Nanowire oxidation directly on the growth substrate was avoided. Since the nanowire density is high and they are in physical contact to each other, oxidization leads to a fusion of nanowires. Instead, oxidation is carried out directly on the later sensor chip substrate after contact printing transfer. Prior to the oxidation the AuSi particle head is removed by immersion in aqua regia acid

(HNO_3/HCl 1/3 v/v) for 2 h. This is essential to avoid a temperature activated Au diffusion in the nanowire during oxidation and prevent Au contaminations of the equipment. The chip is cleaned afterwards in DI water, acetone and isopropanol. For the strong adhesion on the sensor chips due to contact printing most nanowires remain after cleaning procedure. A dry oxidation in a rapid thermal anneal furnace (RTP, AST instruments) follows at 875 °C for 6 min in O_2 atmosphere and a pressure of 1 bar. Subsequent forming gas annealing (H_2/N_2 1/50 v/v) at 1bar and 450 °C for 10 min is utilized to saturate remaining dangling bonds at the Si/SiO_x interfaces [163, 164].

2.2.5 Chip design

The chip mask design comprises lithography patterns for Ni electrodes, top gates and de-passivation layers. The final sensor chip design includes 5 layers

1. Ni interdigitated electrodes
2. windows for etching back oxide on contact pads
3. top gates for test devices
4. passivation layer for Schottky contacts
5. on-chip reference electrode

Mask blanks were bought with pre deposited layers of chromium and positive photoresist (LRC-chromium, AZ 1500 resist) from Rose GmbH. Structuring was done by a laserlithography machine equipped with an interferrometric stage (Heidelberg Instruments DWL 66), development (AZ 350B, Microchemicals) and subsequent etching process (Chromium etch No. 1, Microchemicals). The 4 mask layers are written on the same mask in 2 polarities for both positive and negative resist. In this way the optimal resist can afterwards be chosen and eventual edge broadening and image size augmentation due to sub optimal lithography or etching parameters are the same for all layers.
The transistor devices are realized with interdigitated electrode design fabricated with different inter electrode (IE) length as depicted in figure 2.5. With this design a large area can be used for sensing and many nanowires can be connected in parallel. Single nanowires which are synthesized with length up 40 μm are connected several times by IE pairs. Thus, more than one parallel connected transistor is created by a single nanowire. Test devices and two kinds of sensor devices are patterned on the chip.
The sensor elements are located in the middle of the chip and will be operated with a liquid gate while exposed to an electrolyte (see chapter. 4.1). Therefore, a flexible PDMS stamp with the negative form of a millifluidic channel (dimensions 3 mm width, 18 mm length, 1 mm height) will be force-fitted to the chip surface [165]. In biosensing experiments the main part of the chip surface is covered by PDMS for hydraulic sealing. Thus, long leads to the sensor elements are necessary to enable an electrical connection. Contact pads for electrical connection of the sensor elements are

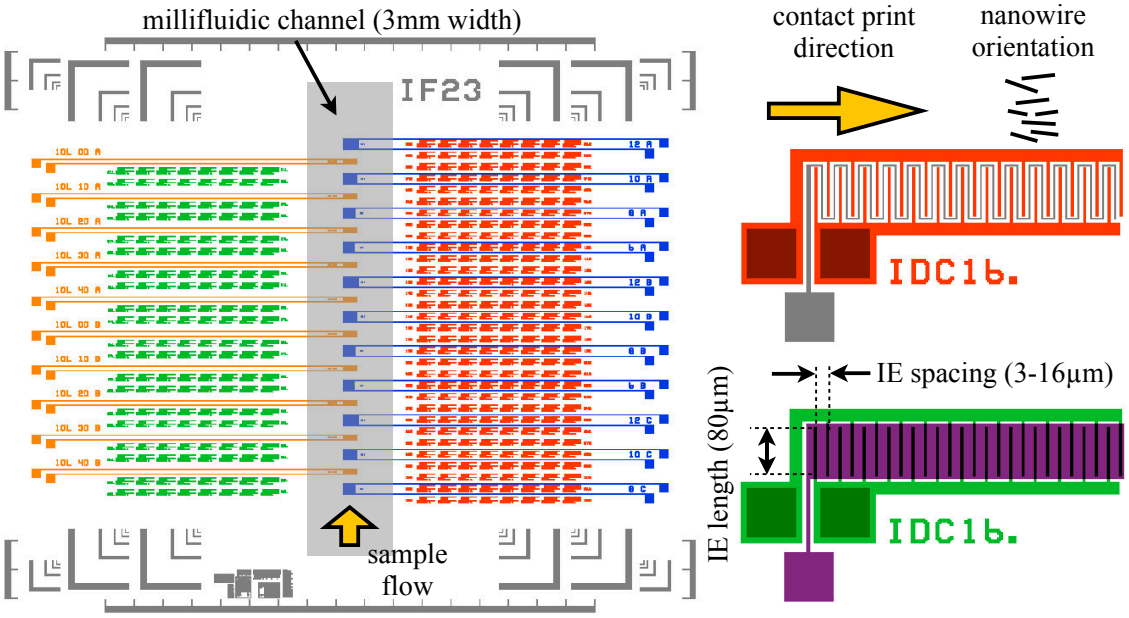

Figure 2.5: Sensor chip design exhibiting four device types with inter digitated electrodes: electrical test devices with various inter electrode (IE) spacings and optional planar top gate (green) or meander shape top gate (red), sensor devices with SU8/Al_2O_3 passivation layer covering Schottky junctions and part of Si nanowire channel (orange), sensor devices with various IE spacings (blue). IE spacings are varied in the range of 3-16 μm. Each transistor exhibits 13 IE pairs (26 electrodes) which are 80 μm long.

located at the chip boundaries far from the middle. The right side connects sensor elements with a series of IE spacings variants ranging from 6,8,10,12 μm. The left side of the chips connects sensor elements with identical geometry and IE spacing of 10 μm. For those devices the passivation layer for the Schottky contacts comes in different sizes (see chapter 5).

The nanowire printing process can lead to scratches along the printing direction and local gate oxide rupturing. Therefore, the electrode design has to be adjusted to minimize the probability of contacting an area with gate oxide defects which would lead to gate leakage. It turned out be essential to orientate the long leads of sensor devices in direction of printing. A lead electrode thickness of 20 μm and length of 1.1 cm was chosen. With the specific conductivity of Ni $\rho = 0.7 - 1\text{x}10^{-7}\,\Omega$m and a deposited Ni electrode thickness of 50 nm this leads to approx. 1 kΩ electrode serial resistance. This is in the same order as the intrinsic transistor resistance in the on state and might limit the sensor output current.

Additionally, 416 test devices in 8 different variants with distinct inter electrode (IE) spacings (3,4,5,6,8,10,12,16 μm) are incorporated. These devices are later used to extract statistical values of transistor parameters and their dependency on IE spacing. The IE are 80 μm in length, 4 μm in width and the IE amount is 26 for all devices. For the small test device structures the electrode serial resistance was calculated to be less than 10 Ω for 50 nm Ni electrode height and is hardly dependent on the IE spacing. Nanowire parallel arrays of nanowire FETs exhibit an intrinsic

resistivity of more than $10^3\,\Omega$ and thus the FET resistivity limits the on-current, as will be shown in chapter 3.

Two top gate variants are included in the mask design for the Al_2O_3 passivated chip. First, top gates in planar all-over geometry for which the whole transistor surface is covered, including nanowires and source drain electrodes. Parasitic capacitances and possibility for gate leakage is high. The situation correlates to the sensor case where the electrolyte covers the entire chip surface within the millifluidic channel. Second, meander shaped gates are fabricated to test the exclusive gating of the inner Si nanowire channel (chapter 5.2). For all IE spacing device variants the meander gate is $2\,\mu$m in width and located in the middle between source drain electrodes.

2.2.6 UV lithography

To pattern the electrodes and openings in the Al_2O_3 passivation layer, UV-lithography is employed. Here, AZ5214e from Microchemicals is used as photo resist. This resist can be employed as positive as well as image reversal resist. Image reversal resist was used to obtain undercut edges for lift-off technology. Exposure and mask layer alignment was done with the mask aligner model MJB4 from Süss Microtec. AZ5214e deposition was done via spin coating (3400 rpm, 1 min) followed by a bake step on a hot plate which leads to an approx. $1\,\mu$m thick resist layer. The process parameters were optimized for accurate structural images and an appropriately high undercut which makes liftoff possible for sputter deposition of metals. Exposure is done for 1 s followed by a postbake (120 °C 2 min) on a hotplate to polymerize the exposed areas. Those areas exhibit cross links which cannot be photo cleaved with the same wavelength again. Finally, a flood exposure for 30 s decomposes areas which were not cross linked before. A development step in AZ 760 MIF (60s) solved resist monomers. After development, a postbake at $120\,^0$C for 4 min is performed to harden the resist and make it more resistive and impenetrable for HF acid, keeping in mind the following etching step. The resist can endure 4min etching in 1% HF.

For back etching of the Al_2O_3 layer, AZ5214e was processed like a positive resist to avoid undercut etching intentionally. Therefore development (AZ 760 MIF, 60s) was performed directly after the first exposure (3 s duration). Afterwards the layer was hardened again on a hotplate at 120 °C for 2 min.

For Schottky junction passivation, SU8 negativ resist was spin coated with 2000 rpm for 1 min, post baked on a hotplate at 60 °C for 4 min then heated to 95 °C for 10 min. The UV-light exposure time was 2 s, subsequently post baked again on a hotplate at 60 °C for 4 min, heated to 95 °C for 10 min., developed in MR 600 DEV for 1 min, and finally hardened on hot plate at 150 °C for 5 min then 30 min in ATV2 at 300 °C in forming gas.

2.2.7 Oxide removal and metal deposition

The UV-lithographic patterend chips are immersed in 1% HF for 80 s to remove the thermally grown nanowire oxide shell locally prior to Ni deposition. The AZ5214e resist layer protects covered areas from the acid for several minutes. The etching solution diffuses into the resist layer and the photo resist layer is lifted for longer etching durations. Therefore, the resist layer thickness and hardening by post anneal have to be adapted to the desired etching times. For less than 3 min etching time 1 μm and postbake at 120 °C for 4 min was found to be sufficient.
Metal deposition was done via sputter coating. The sputtering chamber (Gatan, ion beam coater model 681) used in this work has a load lock, which allows the main chamber to operate permanently in vacuum conditions. Therefore transfer of freshly etched samples to the vacuum chamber is fast (2 min). This prevents the re-oxidation of the nanowire surface. Since the sample is located close to the sputter source, the incident material beam is not focused. The angle variations of incoming material lead to edge coating of conventional photo resists. Then, lift-off is not possible since material layer is closed and the solvent cannot attack the photo resist. In contrast, undercut edges of image reversal resists enable a liftoff technology. However, the undercut presents disadvantages as well. Beneath the undercut edges the nanowire oxide shell is removed as well during HF etching. Moreover, a half shadow like material deposition leads to an undefined material thickness in this area after sputtering. This results in an irregular IE spacing which may vary within the structure. For fabricated transistors, the thermally grown oxide shell may be missing close to the Schottky interface, leading to unipolar devices for an unoptimized process. The image reversal photo resist recipe mentioned above lead to 500 nm undercut in average. By silicidation the source and drain contact should be intruded beyond the undercut determined edge.

2.2.8 Nanowire silicidation

Silicidation is the term for alloy formations of metals and Si. In this work Ni is used as metal. The $NiSi_2$ phase has a very lattice mismatch of 0.4% and forms very sharp interfaces to Si [166]. For silicidized nanowires with $NiSi_2$-Si junctions, atomically abrupt interfaces were observed [167–170]. The nanowire diameter hardly increases by $NiSi_2$ formation. Silicidation decreases the contact resistance significantly (see chapter 3). The axially intruded contacts form metallic tips which lead to a local electric field enhancement at the Schottky junction. This in turn results in a better gate coupling and Schottky barrier thinning, increasing the SB-tunneling probability [97]. Silicidation is performed via forming gas anneal (H_2/N_2 20/1 v/v) in a rapid thermal processing (RTP) furnace at 500 °C. Heating ramps for heating to and cooling from the peak temperature plateau have a slope of approximately 10 °C/s. Prior to $NiSi_2$ formation, Ni rich phases are generated [171, 172]. As mentioned before, those have a lower resistivity but exhibit higher interface roughness

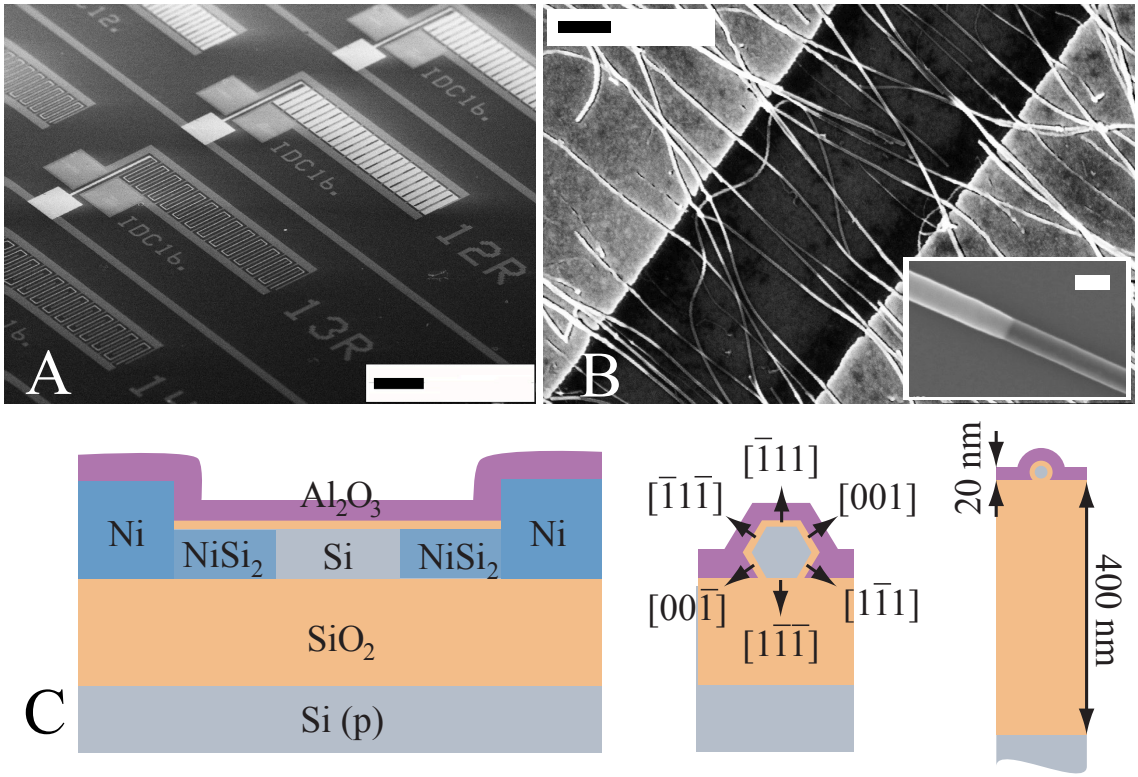

Figure 2.6: Illustration of nanowire parallel array devices with schematic cross section: A) SEM image of top gate devices with meander shaped gate (scale bar 50μm). B) Contacted nanowires (SiNW) for a back gate device (scale bar 1μm). Brighter parts are Ni silicidized phases of the nanowire. Inset shows the (up to) atomically abrupt phase transition between metallic $NiSi_2$(bright) and Si (dark) (scale bar 20nm). This interface poses very defined low defect Schottky junctions. C) left: schematic cross section of the gate stack Si(p-doped degenerately)/SiO_2 back gate oxide/SiNW/SiO_2 shell/Al_2O_3, middle: view along SiNW longitudinal axis (crystal growth direction <110>) with indicated surface planes [90], right: gate stack with actual thickness ratios of layers.

compared to $NiSi_2$ [173]. Rough interfaces create local electrical field enhancement and interface states, which leads to local variations of SB heights and degrade SB-FET performance [80, 174–176]. Temperatures above 450 °C can lead to the formation of the $NiSi_2$ phase. On the other hand, when performed in forming gas, this leads additionally to a hydrogen passivation of dangling bonds at the Si/SiO_2 interface [164]. Therefore, electrical characteristics are improved. Reaction kinetics and silicidation rate change with nanowire crystal orientation [177]. Surface diffusion of Ni on the nanowire was reported to be the dominant diffusion mechanism [168]. In this case, a high surface to volume ratio leads to a fast silicidation. However, the silicidation rate was found to be limited by an interface reaction, i.e. dissolution of Ni in Si at the contact interface [167]. In this case the silicidation rate might increases with growing diameter and nanowire surface area covered by the on top fabricated Ni electrode. The length distribution of nanowire segments under the Ni contacts may have a bigger impact on the silicide length distribution than the nanowire diameter. In figure 2.3 the length distribution of silicidized segments for 30 s forming gas anneal at 500 °C

is shown for nanowires with native oxide shell. For 30 s silicidation duration, all 3 μm and 4 μm IE spacing devices exhibit a fraction of metallic fully silicidized nanowires[2]. This can be easily attested by the device transfer characteristics. A single fully silicidized nanowire was measured to exhibit a resistivity of approximately 200 Ω independently on the gate voltage V_g. Devices consisting of only semiconducting nanowires show a resistivity minimum of more than 1 kΩ and a current modulation with V_g. The upper end of the silicidation length distribution can thus be judged by the electrical characterization as well. It turned out the silicidation rate is smaller for thermally grown nanowire oxide shell, but was not quantified further. For 30 s silicidation of nanowires with thermally grown oxide shell, all devices with IE spacing larger than 3 μm showed FET typically transfer characteristics without occurrence of metallic fully silicidized nanowires.

2.2.9 Ionsensitive, top gate dielectric and contact passivation

Ni electrodes have to be passivated by a protection layer to prevent electrochemical degradation. Photoresist layers, i.e. SU8, which are reported in literature to passivate the contacts, were tested but showed insufficient passivation effect for our devices. Secondly, the thermal Si oxide shell of the nanowires is regarded as a bad ionsensitive dielectric. Alkali metals like K and Na can easily diffuse in SiO_2, which was shown to lead to a hysteretic behavior in pH measurements and drifts [137, 178]. A 20 nm thick Al_2O_3, known to be an ion diffusion barrier for common ions and water in physiological electrolytes, allows to prevent ion related drift effects and passivate the Ni electrodes at the same time [179]. Therefore the sensor chip is completely covered with a 20 nm thick Al_2O_3 layer, made by atomic layer deposition (ALD). The electrodes are covered to prevent electrochemical degradation and leakage currents. The nanowire is covered to increase pH sensitivity and prevent long term drifts due to ion incorporation in the Si oxide. Al_2O_3 shows an excellent and linear pH response because of its high density of hydroxyl (OH) surface groups [67, 135]. This is beneficial for oxide chemical modification with silanes too, which is needed for bio receptor attachment.

The ALD process is an ozone asisted deposition with Tri Methyl Aluminium (TMA) as precursor [180–182]. The process was performed in 150 cycles at 150 °C with the following step parameters: introduction of TMA for 0.35 s, purging for 0.75 s, ozone (O_3) introduction and reaction for 15 s, purging for 10 s. The Al_2O_3 layer is locally back etched at the electrical contact pads by UV-lithographic patterning (positive resist AZ5214e, 1 μm height, post baked for hardening at 120 °C for 2 min) and immersion in 1% HF etchant for 2 min.

[2] By raising the source to drain voltage above 7 V metallic nanowires can be selectively molden.

2.2.10 On chip reference electrode

The construction of a Ag/AgCl reference electrode was explained in [131]. Here, we deposited a hook shaped Ag electrode by UV-lithography and Ag evaporation. A droplet of 1 M KCl is deposited on the electrode with a Pt counter electrode introduced from the top. AgCl is electrochemically formed when applying a constant current (regulated by the power source) of 1 μA for approx. 2 min. The AgCl completely covers the Ag electrode which is later on exposed to the sample solution. The device can be controlled with the Ag/AgCl stack when applying a voltage, although the potential does not seem very stable. Furthermore the AgCl layer is being dissolved over time in solution. For a better electrode stability, KCl gel can be deposited on the Ag/AgCl stack [183]. The criteria for a second order reference electrode are not fulfilled since the Ag/AgCl is not operated in saturated KCl solution. Nevertheless the ISFET can be gated by the Ag/AgCl stack, even in buffer solutions not containing Cl ions (i.e. phosphate buffer). The on chip electrode was not used for experiments described in this work, but can be useful for experiments where the reference electrode has to be close to the FET structure, i.e. digital droplet microfluidics or flexible biosensorics.

3 ELECTRICAL CHARACTERIZATION

This chapter focusses on the nanowire transistor performance analysis. Transfer and output characteristics are presented together with a detailed statistical study of nanowire length dependent device parameters. Further, it is shown how the surface can affect the hysteresis and device performance for passivated and non-passivated devices under different environmental conditions. Differences of back and top gated devices are pointed out. Transfer characteristics reveal the current modulation upon surface potential change. Therefore, they predict the expected signal heights for the pH sensor. Output characteristics show the quantitative scaling of the transistor output current with source/drain voltage. Finally, the transconductance are compared with current noise to estimate the regime for highest signal to noise ratio.

3.1 ELECTRICAL CHARACTERIZATION METHODS

Measurements of back and top gate devices were performed with a Keithley Parameteranalysator 4200-SCS on a Microtec Süss PA200 Probe station with EMI shielded housing. Each of the four source measurement units (SMU) of the Keithley 4200 measurements system is equipped with a preamplifier with a resolution of 10 fA for current measurements. Characterized chips are vacuum force fittet to the probe station chuck [1]. The substrate, i.e. back gate potential is regulated over this chuck. The Si chip substrates are degenerately doped (metallic conductivity) to minimize the space charge region under the back gate oxide and resulting serial capacitance. Transfer characteristics are obtained by V_g sweeps from unbiased condition $V_g = 0V$ (for least electrical stress) to negative, then to positive values and back to $V_g = 0V$, while V_{ds} is kept constant[2]. Cyclic sweeps are performed to study device hysteresis. Also for output characteristics,

[1] motor driven movable gold plated aluminium sample holder with vacuum suction

[2] As mentioned in chapter 1.2, the convention used is: $I_{sd} = I_s - I_d$, $V_s = 0V$, $V_{ds} = V_d - V_s$, $V_{gs} = V_g - V_s$.

a forward and backward sweeping was performed. Voltages are always applied in step functions (no pulsing) and sweeping rate is approximately 1 V/s in average. Gate currents were always recorded during measurements. Measurements were only considered for gate leakage currents below 1 pA. Measurements were commonly performed in ambient air. For individual experiments, N_2 purging was employed to avoid H_2O adsorption as will be pointed out in text below.

3.2 TRANSFER CHARACTERISTICS

The transistor transfer characteristics show the source/drain current I_{sd} as a function of the gate voltage V_g. The appearance of the transfer function and possibility to modulate the current is strongly determined by the electrostatic gate coupling κ. In turn κ depends on the geometry of the transistor, especially the gate oxide thickness and quality. The presence of charges within the dielectric and interface to the semiconductor affects the electrostatic behavior and flatband voltage V_{FB}. Depending on the quality of the dielectric, the density and redistribution of those charges can be affected by the gate voltage cyclic sweeps (see chapter 3.3).

Figure 3.1 shows a comparative overview of transfer characteristics of the different systems characterized in this work, highlighting the impact of gate geometry and oxide quality. On this basis, the measures that were taken to improve the transistor performance can be explained. The characterized device types were:

1. single nanowire devices with native Si oxide shell, back gated
   degenerately p-doped Si/ 20 nm SiO_2 back gate stack
2. nanowire parallel array with native Si oxide shell, back gated
   degenerately p-doped Si/ 400 nm SiO_2 back gate stack
3. nanowire parallel array with thermally grown Si oxide shell, back gated
   degenerately p-doped Si/ 400 nm SiO_2 back gate stack
4. nanowire parallel array with thermally grown Si oxide, top gated
   degenerately p-doped Si/ 400 nm SiO_2 back gate stack and 20 nm Al_2O_3/Ni/Pt top gate stack

All depicted devices underwent a nanowire contact silicidation process as described in chapter 2.2.8. Single nanowire devices (1) with a native oxide shell were measured on a thin (20 nm) back gate Si oxide. The current can be modulated efficiently for the p-branch giving an on/off ratio of over 10^6. Nevertheless the transfer function is shifted towards positive voltages and n-conduction is suppressed. For sweeps to higher positive voltages, the n-branch flattens and saturates fast. Therefore, the transfer function appears asymmetric and is of unipolar p-type. The low quality of natively grown oxide on the nanowire surface is made responsible for this behavior. Water related

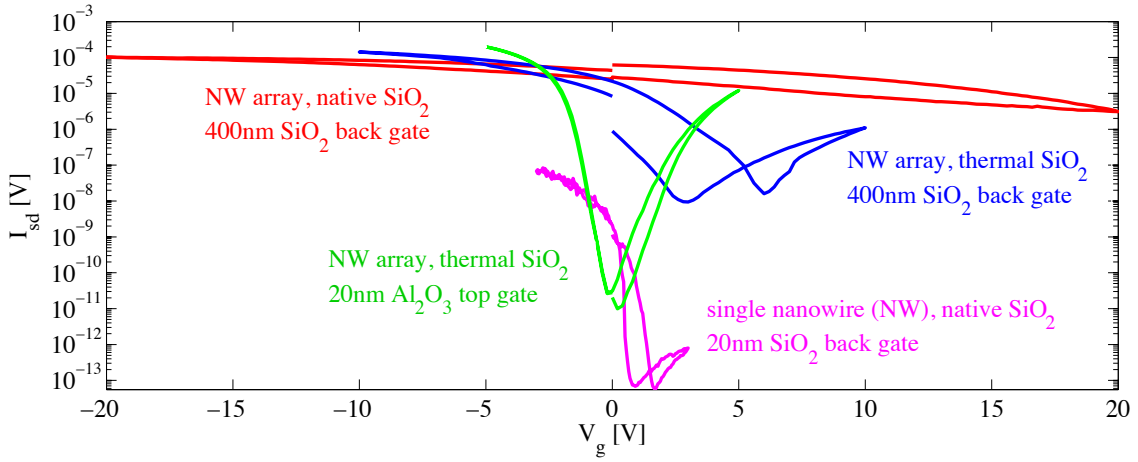

Figure 3.1: Impact of electrostatic gate coupling on the general appearance of the transfer characteristics (recorded for $V_{ds} = -0.5V$) and current modulation capability of the gate: Single nanowire devices with native oxide shell on 20 nm SiO_2 back gate oxide (pink) show suppressed n-conduction. Nanowire parallel arrays with native Si oxide on 400 nm SiO_2 back gate Si oxide (red) have extremely low gate coupling. The current can hardly be modulated. Thermally grown Si oxide shell nanowire parallel array devices on 400 nm SiO_2 back gate oxide (blue) show increased gate coupling. Devices with additional top gate 20 nm Al_2O_3 (green) show enhanced gate coupling and high on/off current ratio. For all devices charge trapping at low frequencies and related hysteresis predominantly occurs for positive V_g and reduces n-currents.

charge trapping for positive gate voltages is proposed as mechanism and is discussed in chapter 3.3.2.

Fabricated nanowire parallel arrays (2-4) generally exhibit approx. 1000 times higher on p-currents than the single nanowire devices. This is in agreement with the finding of approximately 500-1000 nanowire transistors contacted by inter digitated electrodes. Nevertheless, the shape of the transfer function depends on the type of gate and gate dielectric. Parallel arrays of nanowires have to be fabricated on thick back gate oxide to avoid current leakage for the reasons mentioned in 2.2.3. The thick oxide (here 400 nm) reduces the back gate coupling, i.e. effectiveness.

Nanowires with native Si oxide shell have a deficient dielectric layer in between the thermally grown SiO_2 back gate dielectric and Si channel. This layer exhibits an unfavorably high density of charge trapping sites and possible incorporations of water within the layer [184, 185]. This deficient dielectric layer poses a serial capacitance degrading the effective gate capacitance and coupling further. For those devices, current modulation is hardly possible as can be seen from 3.1. The transfer function is extremely shifted to positive V_g, on/off ratio is low and n-conduction can not be reached. Because of the apparent positive flatband voltage V_{FB}, p-currents are turned on for V_g=0V, a characteristic normally-on device behavior. As will pointed out in this chapter, the high charge trap density of native Si oxide in combination with the back gate geometry is made responsible. Like for all back gated devices, V_{FB} drifts further when sweeping to more positive V_g, leading to a modified shape of the transfer function. This apparent charge retention or trapping related hysteresis and memory effect will be discussed in detail in section 3.3.3. Thermally oxidation

of the nanowires (3) after deposition on the sensor chip leads to an enhanced gate control even for a thick back gate dielectric (here again 400 nm), leading to higher on- and lower off-currents. The n-branch becomes accessible, the transfer function shows the characteristic ambipolar (bipolar) shape expected for intrinsic Si-$NiSi_2$ SB-FETs. Nevertheless, the I_dV_g curve is not centered but shifted to positive V_g with a large hysteresis. Currents and subthreshold slope are still smaller for n-branch than for the p-branch. A top gate approach (4) leads to a high gate effectiveness. The reason is mainly the 20 nm thin high-k top gate dielectric leading to a high top gate capacitance and thus coupling. Devices are usually measured in simultaneous double gate, i.e. top and back gate, configuration mainly to reduce oxide break down probability. [3] Trapped charges on the surface and within the nanowire Si oxide shell are now additionally compensated by screening charge in the top gate. As described in section 3.2.3, V_{FB} is thus less affected by built-in negative charge compared to cases (1-3) with absent top gates. For a sufficient gate control the electric potential can be modulated across the whole nanowire cross section. For top gated devices the transfer function looks like the one predicted by theory: the transfer function is centered (normally off) and a steeper p-branch subthreshold slope with slightly higher on p-currents compared to the shallower n-branch with lower on n-currents is observed (chapter 1.2.6). The gate coupling, subthreshold slope and transconductance are much higher than for back gated devices. The saturation currents do not differ.

3.2.1 Silicidation: intruded silicide contacts

The silicidation process leading to axially intruded Ni silicides and the $NiSi_2$/Si interface results in two orders of magnitude increased output currents. The reasons are greatly reduced contact resistance between inter electrodes and nanowire, Si channel length reduction and improved gate coupling. The transfer functions of back gated nanowire parallel array devices with various inter electrode (IE) spacings are depicted in figure 3.2 before and after Ni silicide formation. Silicidation was thermally activated by a forming gas anneal at 500 ^{0}C for 60 s as explained in 2.2.8. Additional forming gas anneals at temperatures over 450 ^{0}C, intended to drive the silicide phase deeper into the Si channel, were found to impair device performance. On/off current ratio and on-currents severely decreased. Since multiple silicidation processes destroy devices, it was not possible to investigate the effect of gradual shortening of the Si conduction channel (L) on the device performance. Instead, the average performance of devices was studied as a function of the IE spacing for a constant silicidation length l_{NiSi_x}. As shown in figure 3.2, an apparent shift of the transistor off-state to positive voltages and on/off ratio decrease is observed towards shrinking inter electrode spacings (IES). Details on the channel length dependent device performance is given in the next section.

[3] The double side gate architecture leads to a marginal threshold voltage shift compared to the configuration where V_{bg} is fixed at 0V. The slopes are not changed.

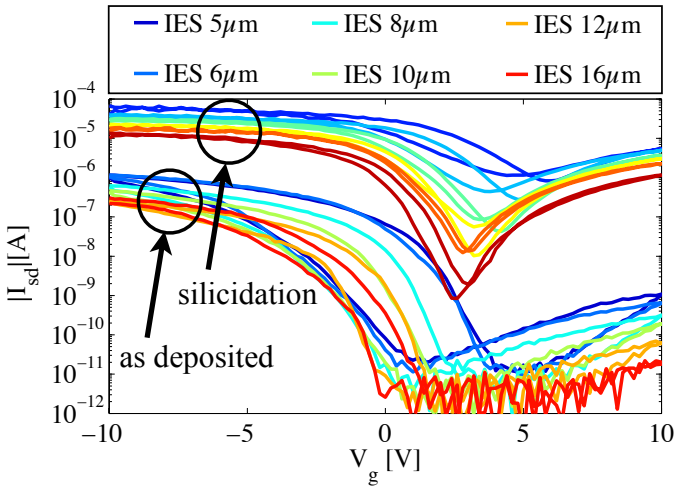

Figure 3.2: Impact of silicidation for various inter electrode spacings (IES). Transfer functions ($V_{ds} = -0.5V$) are depicted before and after silicidation. Silicidation was performed in 1/20 p/p H_2/N_2 at 500 ^{0}C for 1 min. On-currents increased approximately 2 orders of magnitude. Devices with IES of 3 and 4 μm obtain fully silicidized nanowires and show constant currents of over 100 μA independent of V_g (not shown here).

3.2.2 Scaling of the conduction channel length

For different inter electrode (IE) spacings but same mean silicidation length l_{NiSi_x}, a statistical analysis of the transistor parameters was performed. Characterized devices were located on the same chip substrate and underwent the same silicidation process. Thus their mean silicidation length l_{NiSi_x} is equal. The process was a forming gas anneal at 500 ^{0}C for 30 s. The nanowire channel length L, defined as length of the semiconducting Si segment between the metallic silicide phases, is equal to:

$$L = \text{IE spacing} - 2l_{NiSi_x} \tag{3.1}$$

However, l_{NiSi_x} and thus L of individual nanowires within the arrays are statistically distributed like described in chapter 2.2.8. Devices with 3 μm IE spacing obtain fully silicidized nanowires but devices with 4 μm only exhibit semiconducting nanowires. Judged by this result it follows, that the distribution of $2l_{NiSi_x}$ has a maximum value of less than 4 μm but more than 3 μm. The presented statistics on device parameters only contain devices without metallic nanowires (IE spacing>4 μm). Top and back gated devices were characterized. For all devices, nanowires exhibit a thermally grown SiO_2 shell. Back gated devices are fabricated with a 200 nm thick SiO_2 back gate oxide. Top gated devices are fabricated with a 400 nm thick SiO_2 back gate oxide and 20 nm thick Al_2O_3 front oxide with Ni/Pt omega gate.

Figure 3.3 shows representative transfer characteristics of back (A) and top gated devices before (B) and after anneal (C)[4]. For each transistor type a long and short channel device is depicted. After the

[4]Initially conducted as forming gas anneal intented to reduce charge trapping. Indeed, it turned out that annealing in N_2 and forming gas shows the same effects.

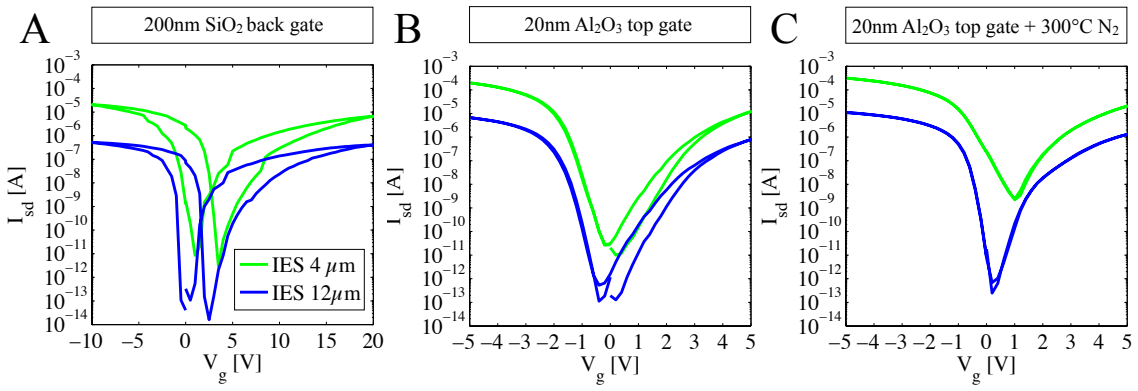

Figure 3.3: Comparison of transfer characteristics of back and top gate long and short channel devices recorded for $V_{ds} = -0.5V$. Interelectrode spacings (IES) were 12 μm and 4 μm respectively. A) Back gated devices, degenerately p-doped Si substrate/ 200 nm SiO_2 back gate stack. B) Top gated devices, degenerately p-doped Si substrate, 400 nm SiO_2 back gate oxide, 20 nm Al_2O_3/Ni/Pt top gate stack. C) Top gated devices after anneal at 300 ^{0}C in N_2 for 10 min. After anneal, device hysteresis vanished, off-region shifted and off-current values increased for small IES.

first characterization of the chip with top gate devices (B), the chip was annealed in N_2 atmosphere 100 mbar at a temperature of 300 ^{0}C for 10 min and characterized again (C). The annealed device statistics show severe influence of post processing on the device parameters. Probably the observed changes after annealing are related to modified lifetime or density of slow charge traps within the gate dielectric (section 3.3.4). A statistical analysis quantifies the dependence of all transistor parameters on the inter electrode (IE) spacing shown in 3.4 for the linear regime, and figure 3.5 for the subthreshold regime. Transistor parameters were extracted from the transfer function recorded at $V_{ds} = -0.5V$. The trends for those parameters are given in table 3.2.2 for back and top gated devices.

As most remarkable difference, large hysteresis and gate voltage needed to transit from the transistor off to on-state is observed for back gate devices. The reason is the 200 nm thick back gate oxide and therefore low oxide capacitance C_{ox} and gate coupling κ. The 20 nm thin high k dielectric and

Transistor parameter	Trend towards decreasing IE spacing	
	back gate/ annealed top gate	top gate
V_g position of min(I_{sd})	shifting to positive V_g	unchanged
min(I_{sd}) = I_{off}	strongly increasing	increasing
max(I_{sd} p-branch) = I^p_{on}	nonlinear increasing	nonlinear increasing
max(I_{sd} n-branch) = I^n_{on}	nonlinear increasing	nonlinear increasing
peak p-transconductance	increasing $\sim I^p_{on}$	increasing $\sim I^p_{on}$
I^p_{on}/I_{off}	decreasing	unchanged
peak p-subthreshold slope	decreasing	unchanged
peak n-subthreshold slope	decreasing	unchanged

Table 3.1: Trends in linear and subthreshold regime towards decreasing inter electrode (IE) spacing for back and top gated devices from parameter statistics 3.4 and 3.5

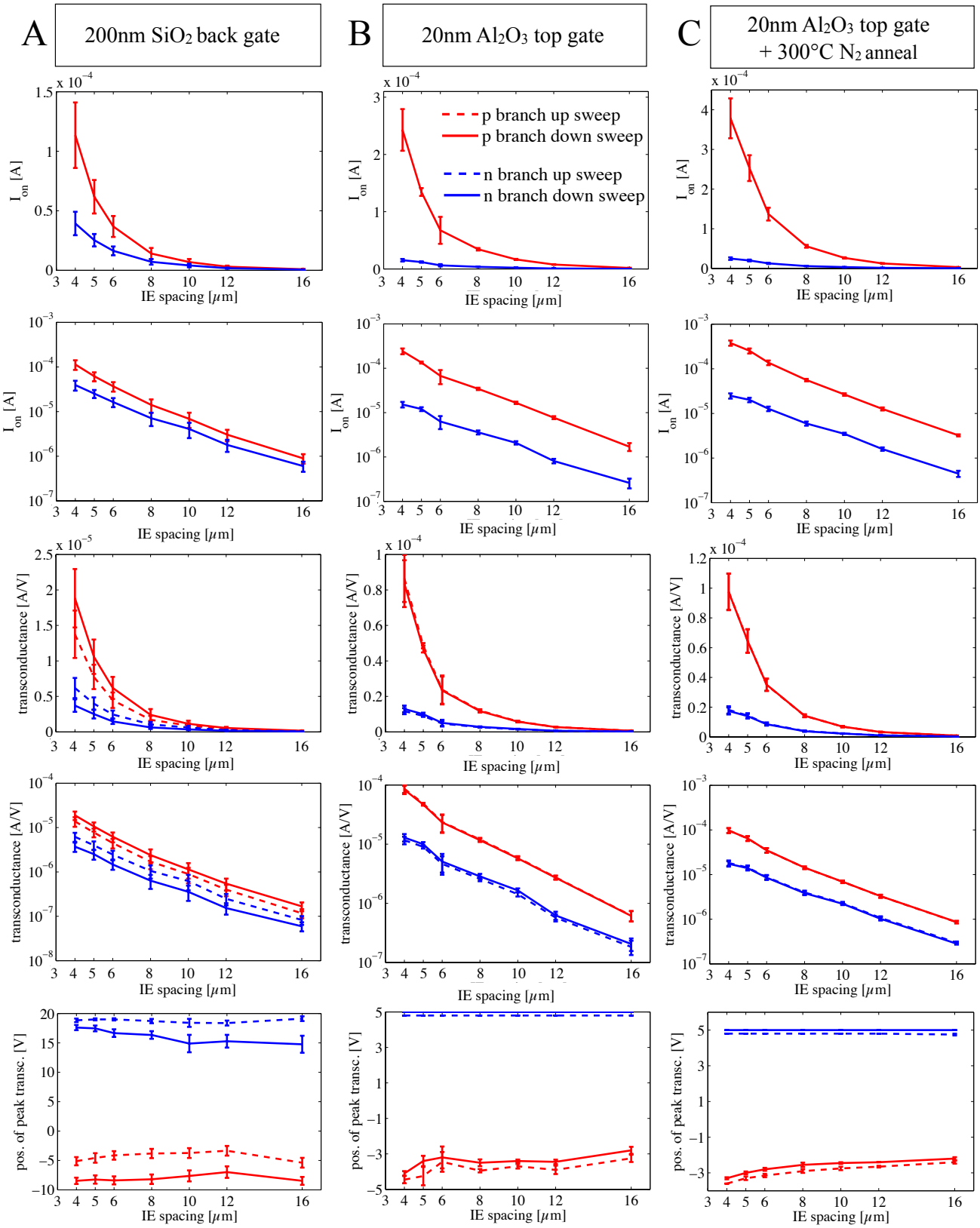

Figure 3.4: Parameter statistics of back and top gate devices in linear regime, extracted from transfer characteristics recorded for $V_{ds} = -0.5V$ (figure 3.3): On-currents are non-linear decreasing with inter electrode (IE) spacing. Peak-transconductance is scaling proportional to on-currents. Position of the peak-transconductance regime is not affected by IE spacing. Difference of dashed (sweep to increasing V_g) and solid (sweep to decreasing V_g) lines show effect of hysteresis.

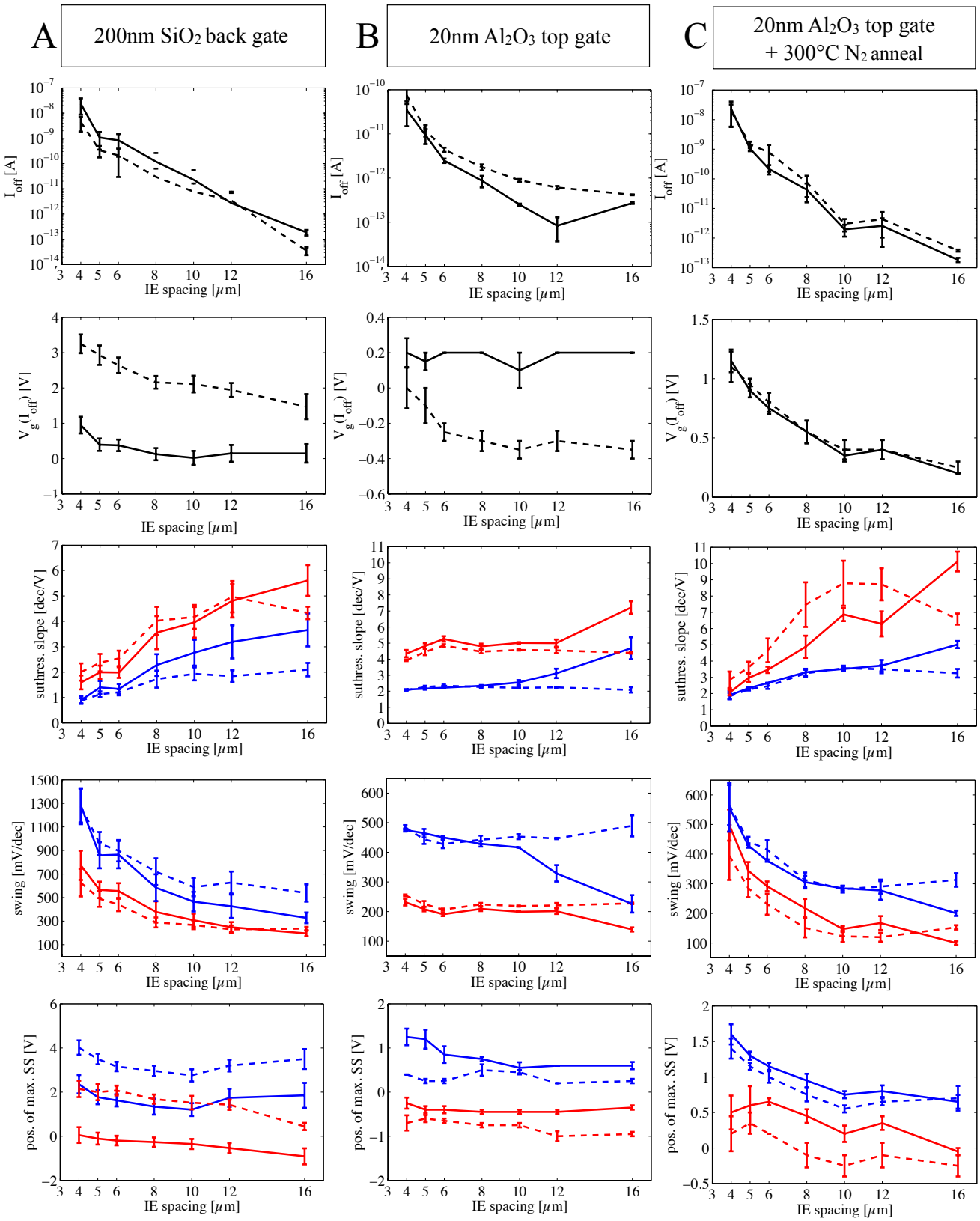

Figure 3.5: Parameter statistics of back and top gate devices in subthreshold regime, extracted from transfer characteristics recorded for $V_{ds} = -0.5V$ (figure 3.3): subthreshold swing (1/slope) degrades, off-current increases for back gated and annealed top gate devices towards small inter electrode (IE) spacings. For top gate devices before anneal, subthreshold swings and off/on current values (compare with figure 3.4) are independent on IE spacing. Difference of dashed (sweep to increasing V_g) and solid (sweep to decreasing V_g) lines show effect of hysteresis. Hysteresis loop direction of top gate devices (cyclic) are inverted compared to back gate devices (anti-cyclic).

omega gate architecture leads to a strong enhancement of κ for top gate devices [186]. Figure 3.4 shows the transistor parameters of interest in the linear regime. Here, maximum n- and p-currents achieved during gate sweep are deliberately defined as on-currents. These currents are actually not saturation currents since the transconductance is not dropping to zero. On-p-currents are a factor 2 lower for back gated devices which can result from fewer nanowires incorporated into the parallel array. However, the different V_g sweeping range makes on-currents not comparable. For both top and back gate devices p and n on-currents and corresponding peak transconductance are increasing nonlinear towards smaller IE spacings. For a linear scaling of the channel resistance R_{ch} with the channel length L one would expect a I_{sd}^{-1} dependency on L. However, the exact mean value of L is unknown but only the IE spacing can be quoted. The flatband voltage V_{FB} seems to shift with IE spacing which additionally influences the on-currents. Taking into account the device geometry (IE width of $4\,\mu$m) and assuming a mean nanowire length of $40\,\mu$m it is assumed that $4\,\mu$m IE spacing devices exhibit 2.5 times more individual nanowire FETs than $16\,\mu$m IE spacing devices. This additionally influences the transistor current scaling. Due to velocity dependent scattering mechanisms, the channel resistivity R_{ch} might also scale non-linear with LEF.

Transconductance $\partial I_{sd}/\partial V_g$ scales similar to the on-current with IE spacing. However, the peak transconductance is 10 times lower for back gated devices because of the lower C_{ox}. Beyond the peak transconductance, $\partial I_{sd}/\partial V_g$ is nearly constant, so the current scales almost linear with V_g. This regime can be called linear regime similar to conventional MOSFETs. For top gated devices peak $\partial I_{sd}/\partial V_g$ values for the n-branch are not reached during the analysis since it appears far in the positive V_g region, where oxide break down is immanent. To prevent permanent damage of the devices this region was not accessed for characterization. However, the maximum $\partial I_{sd}/\partial V_g$ values obtained for the n-branch are depicted here.

Trends for the subthreshold regime, i.e. L dependent subthreshold slope degradation and off region shifts, are substantially different for the three device types (figure 3.5). The smallest obtained (minimum) currents will be called off-currents. The energy bands cannot be flattened at both Schottky interfaces simultaneously by a single gate. P-and n-type tunneling currents can thus not be minimized at once. Therefore, the off-current will depend on how good p- and n- current can be minimized at once by V_g. This strongly depends on the exact potential profile from source to drain and the Schottky barrier heights for holes and electrons (see chapter 1.2.6). For back gated devices and annealed top gate devices, shrinking IE spacing leads to a rapid off-current value increase of several orders of magnitude. The logarithmic value of on-currents increases less and thus on/off ratio decreases. The position for the off-state is shifted further towards positive voltages with decreasing IE spacing. Small spacing devices cannot be turned off efficiently and the subthreshold slopes are degraded. Indeed, the whole transfer function seems to be shifted towards positive gate voltages for back gated devices which implies a positive flatband voltage V_{FB}. For $V_g = 0$V p-conduction is naturally turned on.

In contrast, for top gated devices before annealing the subthreshold slopes and on/off ratio are vir-

tually independent on IE spacing. The transfer functions remain centered, devices are normally off. A predominant charge trapping for positive voltages (negative charge trapping), in the n-branch, is observed though. The n-branch swing is shallower ($\sim 450\,\mathrm{mV/dec}$) than the p-branch swing ($\sim 200\,\mathrm{mV/dec}$). This discrepancy is expected by theory due to the larger Schottky barrier height Φ_{Bn} for electrons but can probably be intensified due to higher charge trapping probability in the n-branch. This is further confirmed by investigations of nanowire devices with native oxide shells, indicating predominant electron trapping (section 3.3.2). Especially in the subthreshold regime, electrostatic coupling seem to be substantially changed after the anneal for top gated devices. Trends of subthreshold slope degradation and off-current increase turn similar to those in back gate devices (see figure 3.5). The hysteresis vanishes completely after anneal in N_2 atmosphere (figure 3.3C). Gate leakage currents remain unchanged by the anneal. Interestingly, the swing degrades for short IE spacings but improves for large IE spacings for both p- and n- branch by the anneal (see figure 3.5).

The significant dependence on device parameters on the IE spacings, i.e. channel length L, can be explained by electrostatic considerations. Electrostatics, i.e. lateral and vertical electric fields, are influenced by the source/drain separation, charges in the dielectric and gate coupling. For shrinking IE spacing, especially increasing lateral electric fields lead to a simultaneous increase of p- and n-current in the off-state and are considered to be the dominant effect. The mentioned effects will be discussed in the following.

• Lateral electric fields:

The intersection point of the p- and n-branch determines the off-current value and position. Especially in the subthreshold regime, the shape of the transfer characteristics depends strongly on the exact energy band (electric potential) progression from source to drain. This in turn is determined by the distribution of lateral and vertical electric fields which scale differently with L. Band bending at source (here $V_s = 0V$) determines the n-current, at drain (here $V_d = -0.5V$) the p-current. For the flatband case $V_g = V_{FB}$, the electric potential in the channel middle is essentially flat but drops at source and drain in opposite directions (see chapter 1.2.6). Bands are bent downwards at source and upwards at drain because of V_{ds}. Therefore, both n- and p-tunneling currents are present. Tunneling currents depend on the lateral electrical field (LEF) at the Schottky contacts (chapter 1.2.5). For shrinking L, the lateral electrical fields (LEF) are overall increasing since V_{ds} was kept at $0.5\,\mathrm{V}$ ($V_{ds} = -0.5V$). This leads to a stronger band bending at the $NiSi_2$-Si contacts, increasing p- and n-tunneling currents at the same time. Therefore, a current increase in the flatband case with shrinking IE spacing is expected. For the $NiSi_2$-Si system, Schottky barrier heights of Φ_{Bp}=0.44 eV, Φ_{Bn}=0.66 eV are assumed [118]. Since Φ_{Bp} for holes is lower, p-current is substantially larger at $V_g = V_{FB}$. As described in chapter 1.2.6, the minimum current, i.e.

transistor off-state, is achieved for $V_g > V_{FB}$: the p-current decreases when V_g is raised to more positive voltages. Although this turns the n-current on, the loss in p-conduction cannot be initially compensated by n-type current increase. Therefore, I_{sd} decreases overall by gating from V_{FB} to more positive V_g. The point where an increase of n-type current is able to compensate the loss of p-type current determines the off-current value and position. This strongly depends on the exact band bending progression which changes according to IE spacing. Both V_g and V_{ds} change band bending at the Schottky contacts. However, the impact of V_{ds} on band bending grows as the channel length L decreases, because the LEF increases. Indeed, larger V_g might be needed to compensate the effect of V_{ds} for small IE spacings. Therefore, the position of the transistor off (minimum) current may be shifted to more positive gate voltages for short channel devices.
Conclusively, the device ambipolarity and complex energy band deformation by the terminal voltages are considered to be the reason for the observed trends in the subthreshold region. The exact scaling of LEF with L might be complicated for nanowire transistors. The intruded metallic $NiSi_2$ contacts have a needle like shape which leads to electric field enhancement at the tip [187]. When the distance L between the tips is reduced, the fringing field components increase and the electrical potential profile from source to drain is distorted. Also the gate coupling factor might be altered with decreasing L and exhibit different values for p- and n-conduction as will be discussed next. Theoretical modeling is recommended for future work to determine the exact potential profile and current transport as a function of device geometry.

• Channel length dependent gate coupling:
Another contribution leading to IE spacing dependent subthreshold slopes, might be a modification of gate coupling factor κ with channel length L. The total front and back gate oxide capacitance scale directly proportional to L. The source and drain capacitances remain essentially independent on L [5]. This might lead to a modified mean value of the channel potential Φ_{ch} within the transistor and terminal coupling factors with varying L. For growing L, the source and drain lose influence on the Si channel. The gate coupling κ in the subthreshold is proposed to be approximated by the ratio of total capacitances of gate oxide C_{ox} to other terminals C_i (see chapter 1.2.2)

$$\kappa \simeq \frac{L(C_{ox}/l)}{\sum_{i=1}^{n} C_i + L(C_{ox}/l)} \tag{3.2}$$

For small L or oxide capacitance per unit length C_{ox}/l this can lead to a L dependence of κ. A low C_{ox}/l is expected for back gated devices and for top gate devices with high parasitic capacitances at the gate oxide, probably generated by charge traps. Classical short channel effects cannot be made responsible for the observations since the channel lengths (L>>500 nm) are far larger than the screening length ($\sim$ 5-10 nm).

[5] Indeed, the depletion layer serial capacitance, i.e. SB thickness, is shrinking with increasing lateral electrical fields

• Asymmetric gate coupling factors for n- and p-conduction:

Many asymmetries are found in the presented system which can lead to a different gate capacitance, and thus coupling for n- and p-branch. For instance, a preferred negative charge accumulation and probably asymmetric D_{it} distribution in the Si band gap. Charge traps can reduce the effective gate capacitance (chapter 1.2.4). Also depletion layer capacitances, which affect the gate coupling, depend on electrical fields and effective masses. Commonly, they differ for p- and n-type charge carriers. Consequently, this leads to unequal gate coupling factors for p- and n-branch (κ_p, κ_n). Furthermore, both coupling factors might change differently with L. If p-branch and n-branch threshold voltage and slope change unequally with L, this could result in a shift of the off-current position and value.

• Effect of N_2 anneal on the transfer characteristics and hysteresis of top gate devices:

N_2 annealed top gate devices show severe changes of the transfer characteristics as described previously. Off-currents increase for small IE spacings, subthreshold swing improves for the n-branch and device hysteresis vanishes while p-branch swing degrades. Improved (degraded) swing for the n-branch (p-branch) would imply a reduction (increase) of electron (hole) charge traps and associated parasitic capacitances. Interface traps with a density D_{it} are fast and lead to a degradation of κ. Since occupation of those trap sites happens on time scales (1-10 μs) much faster than the sweep duration (approx. 10 s), interface traps are not regarded to be responsible for the observed hysteresis here (see chapter 1.2.4). Deep (slow) traps within the bulk of the dielectric layers are commonly regarded to be the reason for charge-voltage hysteresis at low frequencies [101, 103]. Water incorporation in the dielectric is one suggested mechanism producing deep traps [188, 189]. By reducing the inherent molecular water content or densification of the gate dielectric, the amount deep traps might have been reduced by the anneal, which is discussed in section 3.3.4. However, a vanishing hysteresis does not necessarily mean less charge trapping but can result from a modified lifetime of deep traps too (see chapter 1.2.4). Especially for amibolar devices, charge trapping is assumed to significantly affect the appearance of the transfer characteristics. It might be the increased n-current due to a reduction of electron trap sites by device annealing which leads to an off-current increase for small IE spacings. A trap free ambipolar device exhibits high off-currents composed of p- and n-currents naturally. Charge trapping of predominantly one charge carrier type might lead to a better on/off current ratio. This could explain why non-annealed top gate devices, exhibiting charge trapping predominantly in the n-branch, show lower off-currents. Frequency dependent measurements of the gate capacitance are recommended to investigate the impact of parasitic capacitances resulting from charge traps.

Besides, it cannot be excluded that the $NiSi_2$/Si interface was affected by the anneal. Although SEM investigations showed an unnoticeable silicide length increase, an eventual interface rough-

ening would lead to undefined Schottky barriers and local SB height variations. Local field enhancement at spikes on the rough interface can lead to tunneling leakage currents, increasing the off-current. Also a change of the Ni silicide stoichiometry at the junction could result in a modified work function and change the Schottky barrier heights [118, 125].

Conclusively, the transistor subthreshold regime and therefore off-current and on/off-ratio is governed by asymmetric charge trapping and ambipolar conductive behavior. Conduction in the off-state is determined by the electric potential profile from source to drain which is seriously altered by the transistor Si channel length.

3.2.3 Flatband voltage, built-in potentials, fixed and trapped oxide charge

Built-in potentials determine the flatband voltage V_{FB} and therefore the transistor current at $V_g = 0V$. For all back gate devices, p-current is already turned on at $V_g = 0V$, so devices seem to be prebiased due to a positive V_{FB}. This is observed for devices with native and thermally grown nanowire oxide shell, although the effect is especially severe for a native oxide shell. Indeed, the positive V_{FB} was also observed before the silicidation process. The possibilities for built-in potentials are manifold.

First of all, the difference in work function between $NiSi_2$ contact and Si channel leads to a positive prebiasing (see chapter 1.2.5). V_{FB} is gate work function dependent as well. The different flatband voltage V_{FB} of top and back gate can arise from the different work functions of p-doped substrate gate and Ni/Pt top gate. The gate work function leads to a charge exchange of SiNW-channel to gate and therefore to a prebiased channel potential. Additionally, there might be the possibility of charge transfer between the ambient air and the nanowire channel for back gate devices. Although the work function cannot be defined of ambient air, unpassivated Ni electrodes enable chemical reactions which could lead to charge exchange between ambient air and nanowire channel. Nevertheless, the curve shift for charge exchange resulting from different work functions should be independent of L or κ. Indeed, charge transfer from the degenerately p-doped back gate would explain the hole accumulation for back gated devices at $V_g = 0V$. However, nanowire top gate FETs produced on flexible substrates showed a similar V_{FB} leading to normally-on p-current devices. Since the p-doped back gate is missing for these devices, one can exclude this to be the main reason for positive V_{FB}.

Besides, charges within the gate oxide affect V_{FB} like described in chapter 1.2.3. Built-in oxide fixed charges Q_f can result from defects, like oxygen vacancies, in non stoichiometric SiO_2 and were reported to be charged positively [190–192]. However, the presented devices generally exhibit positive V_{FB}, which implies a negative sign of charges within the dielectric. Indeed, V_{FB} drifts further towards positive values during device operation in positive V_g range (see section 3.3.3).

This indicates negative oxide charging, eventually oxide trapped charge Q_{ot} generation induced by electrical stress. Hysteresis investigations on single nanowire transistors with native Si oxide support the assumption of predominant electron trapping with a large retention time (section 3.3.2). These observations suggest, that the stable trapping of negative charge strongly promotes positive V_{FB}, observed for devices with thick back gate oxide and missing top gate (section 3.2.2). How far V_{FB} is affected by the trapped charge is determined by the gate geometry. First of all, for small C_{ox}, large V_g are needed to compensate charge at the interface of Si nanowire and SiO_2 shell (equation 1.12). Trapped and fixed charges can also be distributed around and within the nanowire oxide shell. The physical location of trapped and fixed charge is essential. If a metal gate is fabricated on top of a nanowire transistor, charges close to the interface of the gate side are screened in the gate (see chapter 1.2.3). Generally, built-in charge shows a more pronounced effect on V_{FB} if parts of the nanowire surface are not coupled to a gate which can contribute to screening. For back gated devices, the nanowire surface is facing the ambient air, the metal top gate is missing. Thus, charges within and on the surface of the upper part of the Si oxide shell have to be compensated by screening charge predominantly in the Si channel. In particular for a large ratio of back gate oxide thickness t_{ox} to nanowire Si oxide shell diameter, the back gate contributes hardly to screening of oxide charge as equation 1.12 indicates[6]. This explains the strong positive V_{FB} found especially for back gated devices with thick t_{ox}.

3.2.4 Surface effects on the channel potential of back gated SB-FETs

As mentioned earlier, the thick back gate dielectric lowers the back gate coupling κ significantly. For small κ, other terminals, i.e. source and drain as well as the floating surface potential, influence the channel potential to a large extend. Indeed, simulations for back gated devices showed that close to the $NiSi_2$-Si interface only the lower part of the nanowire, close to the substrate, is efficiently gated. The upper parts are dominated by the $NiSi_2$ metallic contact though, which screens the back gate fields. Thus, the band bending in the upper surface part of the nanowire can look completely different from the bottom part of the nanowire. A fraction of the nanowire cross section could exhibit a conduction path permanently turned on or off. Indeed, all devices show p-conduction for V_g=0 V. The V_{th} shift towards positive gate voltages indicates hole accumulation for unbiased gate. This can arise from built-in negative oxide trapped or fixed charge (see chapter 1.2.3). Thus in the upper nanowire parts, where gate control is lost, p-conduction might be turned on permanently leading to high off currents. Especially for low κ devices, the gate might be only able to turn off p-type conduction in those regions for large positive gate voltages where n-conduction is already turned on in the other nanowire parts. For back gated devices also the floating surface potential

[6]For single nanowire devices shown here, the thin t_{ox} of 10 nm leads to an additional oxide charge screening by the back gate.

can have a substantial impact. The front nanowire oxide shell and ambient air are commonly regarded as pure dielectrics. In reality the surface may carry a net charge accumulated from the ambient or by the metal source/drain contacts. This is not surprising since insulators are known to accumulate surface charge. The accumulated charge can be fixed or mobile. Fixed charge can be a SiO^- group and only shifts V_{FB}. Mobile charges Q_m and adsorbed water lead to a screening of back gate fields and thus a reduction in κ. If there is a time delay of Q_m redistribution according to V_g, hysteresis is observed. Surface conductance in ambient air at high humidity was experimentally verified for inter electrode patterns without nanowires. The surface potential might then strongly be influenced by source and drain contacts. Indeed, in the case of significant surface conductance and charge density, the surface potential is not floating but pinned to source-or-drain potential. Since the nanowire oxide shell is much thinner than the back gate oxide, the coupling to the surface potential is much stronger and dominates the device. Water is known to adhere strongly to oxide surfaces and have a very high impact on the performance of all kinds of nano devices like CNT, graphene, organic and nanowire FETs [193–197]. Water has a strong dipole moment and a dielectric constant of $\epsilon = 80$. Water dipoles can screen electric fields efficiently. Furthermore, water can be a promotor of slow charge trapping [189]. Silanol groups are electrochemically split in presence of water by an injected electron and create negative oxide trapped charge. The effect of water adsorption on the surface is discussed in detail in 3.3.2. Since biased Ni electrodes are exposed to the ambient air, electrochemistry is likely to happen as well. Gas molecules in the air, i.e. water, can be ionized and redistributed over the surface. Such charge transfer was observed for back gated devices between an organic layer and the Ni electrodes [198].

3.3 CHARGE TRAPS, HYSTERESIS AND V_{TH} DRIFTS

In this chapter the effect of charge trapping and charge-voltage hysteresis on the device characteristics is presented. Electrical hysteresis leads to a change of V_{FB} and V_{th}, subthreshold slope and transconductance over time. Since V_{th} is the sensor parameter of interest which reflects the analyte binding and resulting surface charge, measurements are falsified. Charge trapping can result in parasitic capacitances which impair the gate coupling κ. Additionally to the presence of fast interface traps reducing κ, deep (slow) charge trapping is suggested to be responsible for the observed charge-voltage hysteresis. Especially the subthreshold behavior is supposed to be strongly dominated by charge trapping as discussed in the statistical analysis part above. Hysteresis can result from time delay in self charging or dielectric polarization. It behaves very different for top and back gate, native and thermally oxidized devices. A common feature of all device types is a predominantly occurrence of hysteresis for positive gate voltages. This remarkable feature indicates an facilitated negative trapped charge generation leading to a preferred hole accumulation in the nanowire channel. The preferred electron trapping can explain the positive V_{FB} shift of back

gated devices. This asymmetry is pronounced stronger for native oxide nanowire devices and leads to their unipolar p-type behavior. It will be shown that the presence of water promotes hysteresis and might be the inherent reason for unipolarity of native oxide devices. Possible mechanisms are discussed.

3.3.1 Screening of back gate fields by water molecules

Water adsorption leads to enhanced hysteresis as shown by the following experiments. Water is always present, strongly adsorbed on OH containing surfaces. Water was observed to induce hysteresis and charging effects on all kinds of back gated nanostructure devices and vitiate the inherent characteristics [193–197]. Here, water adsorption on Si nanowire back gated devices (SiO_2 200 nm) with a thermally grown Si oxide shell is investigated. Al_2O_3 passivation layer and metallic top gate are missing for the devices. Transfer characteristics were measured in ambient air at room temperature and after gradual cooling down in steps to $4\,^0$C with a temperature controlled chuck. Gradual water adsorption was visible under the microscope while approaching the dew point. Little water droplets condensed at the chip surface at $10\,^0$C. The hysteresis amplitude increased and the direction reversed from cyclic to anti-cyclic. At $4\,^0$C more water adsorbed, the anti-cyclic hysteresis is so strong, that the transfer characteristics are deformed to a cigar like shape. This indicates a retarded screening effect. Two mechanisms are proposed here. Water dipoles can screen the electric fields at the nanowire surface by a retarded polarization induced by the gate. In turn electric fields drop across the Si/SiO_2 interface at the bottom of the nanowire because of the modified electrostatics. Therefore, charge trapping at the Si/SiO_2 interface or at deep traps near this interface is promoted additionally. When the device is heated above $120\,^0$C for 10 min under N_2 purge, the hysteresis vanishes completely but V_{FB} is still permanently shifted toward positive V_g. This indicates remaining negative trapped charge.

A more pronounced screening was observed for O_2-plasma treatment of the device. O_2-plasma treatment is used for generation of hydroxyl (OH) or silanol (Si-OH) groups for later chemical bonding of silanes on the surface [199]. Silanol groups are known to make the surface hydrophilic which results in water adsorption from the air. Plasma treated devices show a complete loss of gate control. Indeed, the current level is pinned to the p-type current at V_g=0V from the initial transfer characteristics. This indicates that the SiNW channel potential cannot be modified by the gate any longer. It also shows, that for a loss of gate control p-type currents are turned on. This will be especially important for the findings shown in chapter 5.2.2 for partially top gated device. The gate controllability is completely regained after surface silanization. Silane attachment leads to a replacement of silanol groups with an organic monolayer. The water, previously adsorbed to the silanol groups, desorbs as well. Here silanization was carried out by immersion in ODTS

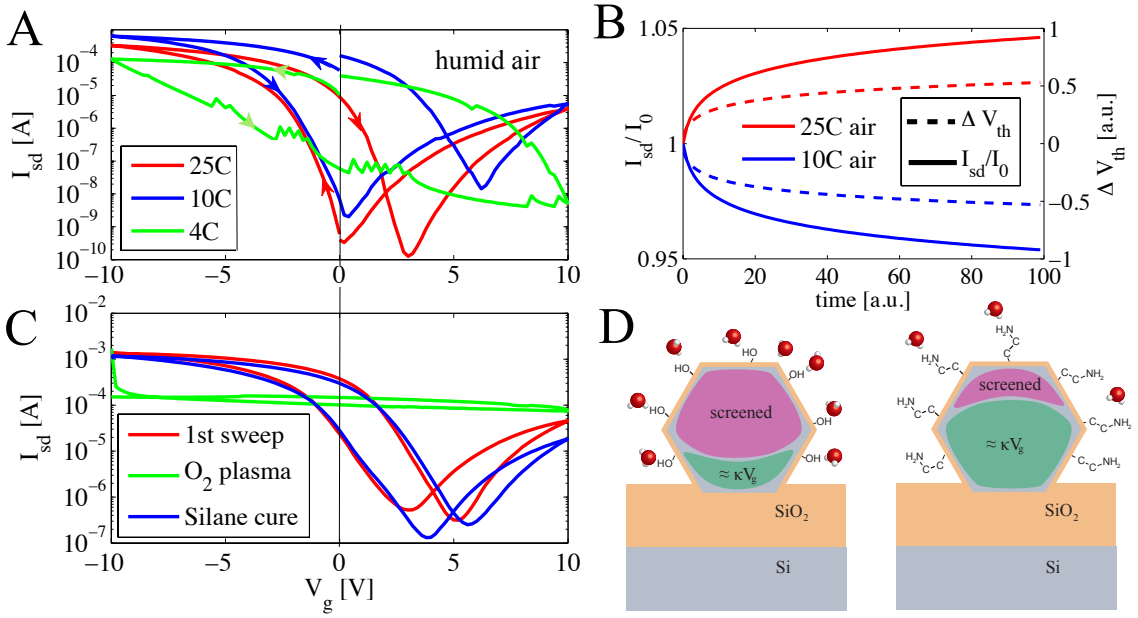

Figure 3.6: Gate coupling loss due to water adsorption for back gated devices without Al_2O_3 passivation layer: A) Water condenses on chip surface in ambient humid air by cooling under the dew point at 10 °C ($V_{ds} = -0.5V$). This causes a reversal of the hysteresis loop direction. At 4 °C the adsorbed water layer screens gate fields efficiently and coupling is lost. This behavior is not observed in dry air. B) Schematic trends of V_{th} and I_{sd} dependence on temperature in humid air from A). At 10 °C V_{th} drifts appear to be positive, current decreases over time for constant voltages (blue). The opposite trend is observed at room temperature (red) since the hysteresis loop direction is reversed. C) Oxygen plasma treatment ($V_{ds} = -0.5V$) leads to surface hydrophilization and water adsorption; gate coupling is lost. Chemical passivation, i.e. replacement of hydroxyl groups with alkanes via silanization at room temperature restores the gate coupling completely. D) Model for gate field screening: hydroxyl groups on the surface lead to hydrophilicity and water adsorption. Probable screening effects, charge trapping or a pinned surface potential result in a back gate decoupling. Alkene-amino groups replacing the hydroxyl groups render the surface more hydrophobic and might reduce water related back gate screening.

(octadecyltrichlorosilane) 0.2% in choloform at room temperature for 2 min. ODTS monolayers are known and were proven to be strongly hydrophobic. Gate control is regained after the treatment. This shows that devices were not damaged by O_2-plasma and that the modified surface state only was responsible for gate control loss. For O_2-plasma treated devices, gate controllability is also regained after exposure to ambient air for a few weeks. During the first few days, the transfer function shows a large hysteresis analogous to the cooled down device with adsorbed water. Hysteresis is more and more reduced over time until the initial appearance is restored.

An alternative explanation of gate control loss is possible enhanced surface conductance [200]. The surface potential would be influenced strongly by the source and drain contacts. Since the front oxide is much thinner than the back gate oxide, the Si channel potential would be strongly determined by the source/drain dominated surface potential.

This chapter shows the strong impact of water on hysteresis and gate controllability for thermally oxidized nanowires, although the exact mechanism could not be derived. Findings presented in the

next chapter indicate, that molecular water, interdiffused into the bulk of the gate dielectric, can produce deep charge traps which lead to hysteresis and unipolar behavior of native oxide nanowire devices.

3.3.2 Native oxides: unipolarity by water promoted charge trapping

Unipolarity and hysteresis was observed for native oxide nanowires before and was associated with charge trapping at the gate dielectric [201]. Also for other transistor systems, unexpected unipolarity is explained by charge trapping [202, 203]. However, the nature and location of those traps is unknown. The Si/SiO_2 interface might have an asymmetric interface trap energy distribution. The energy distribution of D_{it} depends strongly on the crystal orientation (figure 1.3). So it can in principle be possible that unipolarity is caused by inherent charge trapping asymmetry. However, because of the short lifetime of interface traps, they are not expected to cause hysteresis at low frequencies, i.e. retention times of several seconds. Instead, slow charge traps within the bulk of the gate dielectric but close to the Si/SiO_2 interface are commonly regarded to be accountable [101, 103]. A possible mechanism of deep trap generation is related to a chemical reaction in presence of molecular water within the gate dielectric [188, 189]. Water related charge trapping mechanism was also proposed to explain hysteresis in CNTs [193]. Here, the presented results give a strong indication that molecular water and predominant electron trapping indeed cause device unipolarity.

Hysteresis was investigated for a single back gated nanowire device with native oxide shell. Single nanowire devices were produced by spray coating and electroless Ni deposition like described in section 2.1. Figure 3.7 shows the transfer characteristics of the device. The back gate SiO_2 thickness was 20 nm and the channel length 2 μm. Therefore, the gate coupling for the p-branch was high as seen by the high on/off ratio. Nevertheless, the device is unipolar p-type. No hysteresis is observed when V_g is swept from V_g=0V to negative values and back to V_g=0V. As soon as positive V_g is applied and electrons are injected into the SiNW channel, a strong hysteresis is observed. The n-current does not rise but is suppressed when sweeping to increasingly positive V_g. The injected charge appears to be immediately trapped, not contributing to charge transport. The electric gate fields decay mainly over the oxide and not within the Si depletion layer. The subthreshold slope is then determined by a lower effective gate capacitance (equation 1.13). When the gate bias is reduced again towards V_g=0V, detrapping occurs partially. At V_g=0V a certain amount of negative trapped charge is still present. This leads to a accumulation of holes in the adjacent channel and to p-conduction. The negative trapped charge is quite stable and cannot be detrapped by negative V_g biasing again. Indeed, after the first sweep the device turned into a normally on p-type device. The explanation given here is related to charge trapping. Surface adsorbates might have been an alternative explanation. However, since the flatband voltage V_{FB} is shifting to

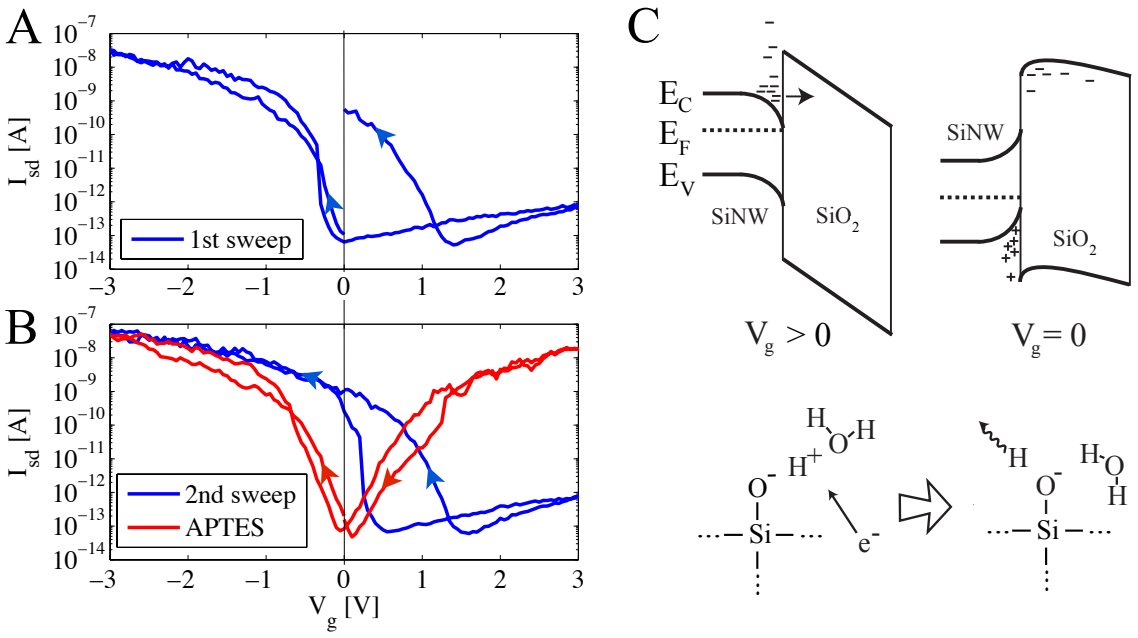

Figure 3.7: Transfer characteristics ($V_{ds} = -0.5V$) of a back gated single nanowire devices with native oxide shell, indicating negative trapped charge generation during V_g sweeps: A) Unipolar p-type behavior is observed. Charge trapping with a large retention time predominantly happens for positive voltage, i.e. electron injection into the Si conduction channel. B) After first sweep to positive V_g, oxide remains negatively charged leading to a modified V_{th} for subsequent sweeps (blue curve). Sweeps to negative voltages do not result in charge detrapping, V_{th} remains modified. Surface passivated devices (red curve) show ambipolar transfer characteristics. Passivation was achieved by surface silanization with (3-Aminopropyl)triethoxysilane (APTES) at room temperature, creating a hydrophobic nanowire surface while additionally consuming H_2O in the reaction. C) Negative oxide trapped charge Q_{ot} generation for sweeps at positive gate voltages is assumed to cause charge trapping asymmetry behavior. An irreversible reaction of electrons with inherent water is proposed as mechanism for oxide charging.

positive voltages, this indicates negative charging. Surface adsorbates would have positive charge when the channel is filled with electrons for positive V_g. Therefore surface adsorbates are excluded as possibility for the V_{FB} shift.

A complete reshaping of the original transistor transfer function could be achieved only by a chemical modification of the nanowire surface (see figure 3.7B). After electrical characterization, revealing unipolar characteristics, the devices were functionalized by immersion in an ethanol solution containing 0,2% (3-Aminopropyl)triethoxysilane (APTES) at room temperature. This surface modification replaces the OH groups by SiC_3NH_2 at the surface (groups which can be cross linked to each other) which renders the surface more hydrophobic. After the surface treatment a change of the transfer function to ambipolar can be observed. The n-currents increase by 4 orders of magnitude and the curve is centered. The on-currents for p-type are not changed after functionalization. The I_dV_g appearance is close to one predicted by SB-theory. This all was achieved by a surface reaction at room temperature. The Si/SiO_2 interface states are not expected to have been modified. But indeed the water adsorption is prevented by APTES monolayers

which was shown to suppress device hysteresis [194, 204]. Additionally, the silane binding reaction consumes water which might reduce the water content within the amorphous SiO_2 nanowire shell. This might reduce the density of deep traps which are produced by molecular water as will be explained in the following.

The strong trapping in n-branch accompanied with V_{th} shifts and n-current suppression seems to be a water related effect. The extreme asymmetry poses the question what the exact mechanism is for electron trapping. Although many groups discuss water dipole reorientation to cause hysteresis [204, 205], for this particular system of undoped nanowires with native oxide another mechanism is proposed here. Since trapping at low frequencies essentially only occurs for positive V_g and trapped charge is very long time stable, water related electron trapping is proposed as mechanism [188, 189]. Native oxide is known to be porous, hygroscopic and be able to swell by water incorporation [206–208]. As a low quality insulator, leakage currents are thus likely to happen. Water from the nanowire surface or negative charge from the channel side can diffuse into the amorphous SiO_2. Water molecules form negatively charged SiO^- sites within the amorphous oxide layer with embedded hydroxyl groups by a semi-reversible reaction [188].

$$SiO^- + H_3O^+ + e^- \rightarrow SiO^- + H_2O + H \tag{3.3}$$

Electrons are needed for the reaction and water has to be present. In this setup, this would imply, that the reaction only happens for positive V_g, when the nanowire channel fills with electrons. For the H atom diffusing away, the reaction is quasi irreversible. This reaction consequently creates oxide trapped charge Q_{ot} within the bulk of the gate dielectric. Further, a low gate dielectric insulation quality (i.e. low resistivity), like it is the case for native Si oxides, facilitate Q_{ot} generation without the need for hot electrons (i.e. high electric fields).

The proposed model explains the observed behavior of charge-voltage hysteresis and unipolarity very well. Unipolarity of undoped SB-FETs was also explained by interface states at the metal-semiconductor interface (MIGs) or incorporation of Au atoms acting as p-type dopant [209, 210]. Since we changed the transfer characteristics to amibipolar by a process at room temperature, not enabling structural changes in the nanowire but only modifying the surface, one can exclude this explanations for our system.

3.3.3 Hysteresis for thermally grown oxide back and top gate devices

For back gated devices a positive flatband voltage V_{FB} is present from the beginning. This leads to a turned on p-conduction for $V_g = 0V$ and is observed for devices with and without Al_2O_3 top gate dielectric. However, device transfer characteristics are drifting even further towards positive voltages by electrical stress. The curve shift is strongly increased when high positive V_g values are applied depicted in figure 3.8. A saturation has not been observed. Indeed, V_{FB} shifts further in

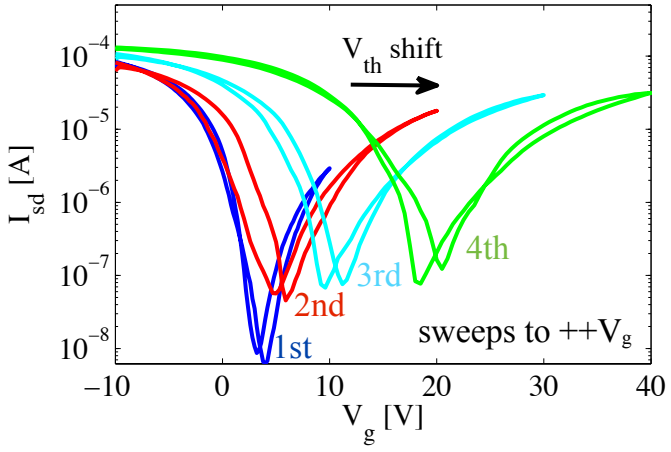

Figure 3.8: Threshold voltage V_{th} dependence on electrical stress, recorded for $V_{ds} = -0.5V$: Before each gate voltage sweep was performed, a constant gate voltage is applied for 5 s at the highest positive value of the respective scan range (1st=+10V, 2nd=+20V, 3rd=+30V, 4th=+40V). Apparently, the electrical stress induces negative trapped charge shifting the flatband voltage V_{FB} towards more positive voltages. Back gated (t_{ox} 200 nm SiO_2) device does not exhibit a Al_2O_3 top gate dielectric layer.

the positive V_g range as V_g is increased in positive direction. The shift is quasi permanent, which means that V_{FB} remains shifted also when the V_g sweeping range is decreased again. The retention time of this V_{FB} shift is in the range of several days. The strong and permanent shift indicates oxide trapped charge generation or trapping in deep trap levels. However, this additionally introduced immobile negative oxide charge does not affect the subthreshold slopes, although off-currents are increasing marginally. P- and -n conduction can still both be achieved. For thermally oxidized nanowires with top gates, one can still observe a higher hysteresis in the n-branch than in p-branch. Hysteresis is much more pronounced for back gated devices without top gate though. This arises mainly from the lack of the metallic top gate, which would contribute to the screening of charges within the dielectric: all charges in the Si nanowire oxide shell are screened almost exclusively in the Si conduction channel since the back gate oxide thickness, with 200-400 nm, is very large (equation 1.12). Annealed top gate devices show no hysteresis anymore. The reason can be a modified trap charge lifetime or a reduction of water content in the Si oxide dielectric discussed in the next chapter.

3.3.4 Hysteresis reduction by post anneal

Top gate devices show a substantially decreased hysteresis after anneals at 300 ^{0}C in forming gas or nitrogen atmosphere. Adsorbed water has been shown to have a serious impact on charge trapping. Before anneal, devices showed a preferred charge trapping at positive gate voltages. For both back and top gated devices it was observed that anneals over 100 ^{0}C can reduce hysteresis significantly. The N_2 anneal might have reduced the water content within the dielectrics. This in turn would

have reduced the amount of water related electron charge traps. In consequence, this can explain the hysteresis reduction for positive V_g and increase of n-type currents after anneal.
Alternatively, the charge trap lifetime τ_{ot} could have been modified by the anneal. If R_{ot} is lowered, for instance by a degradation of the insulation quality of the gate oxide, leading an increase of leakage current from Si channel to the gate leakage, the occupation rate for charge trapping would increase. In this case trapping can follow V_g for slow V_g sweeps and no phaselag and thus no hysteresis is observed any longer (see chapter 1.2.4, figure 1.3). Consequently, the gate coupling κ is reduced according to equation 1.13. If charge trap lifetimes τ_{ot} increased by the anneal, hysteresis could be reduced, accompanied with an increase of κ.
Further, Si/SiO_2 or SiO_2/Al_2O_3 interface traps could have been affected by the anneal. Depending on the energy distribution of D_{it} and charge neutrality level CNL, the flatband voltage is changed. For a CNL below the Si midgap, energy bands are bent upwards at the nanowire surface and positive charge accumulates in the channel. Depassivation of charge traps was reported to be possible depending on annealing conditions [211]. Nitrogen anneal could eventually depassivated charge trapping sites at the Si/SiO_2 interface and lead to a modified CNL and larger D_{it}, C_{it} [108]. This could explain the observed modified flatband voltage and diminished swing (for small IE spacing devices).
The exact mechanism of hysteresis reduction can not clearly be assessed in this work. However, the previous observations of water, strongly promoting hysteresis, justify the explanation of density reduction of deep traps by removal of molecular water within the dielectric layer. Further investigation like charge pumping technique and voltage-capacitance (CV) measurements are recommended [huang2003electron , 212, 213]. However, the experiments show that post-processing can potentially inflict severe changes in charge trapping properties, hysteresis and parasitic capacitances. The appearance of the transfer characteristics are strongly influenced by charge trapping.

3.4 OUTPUT CHARACTERISTICS

The output characteristics I_{sd} vs. V_{ds} are presented here first for nanowire parallel array back gate devices with native Si oxide shell and second for top gate devices with thermally grown Si oxide shell.

3.4.1 Unipolar output characteristics of nanowires with native oxide shell

The characterized device has a 100 nm thick back gate oxide, Si nanowires with native oxide exhibit 500 nm channel length L. A decent current modulation with the back gate was possible as shown by the transfer characteristics (inset figure 3.9). Charge transport was blocked for positive V_g, p-currents turned on for negative V_g, the device is normally off. For negative V_g, the native

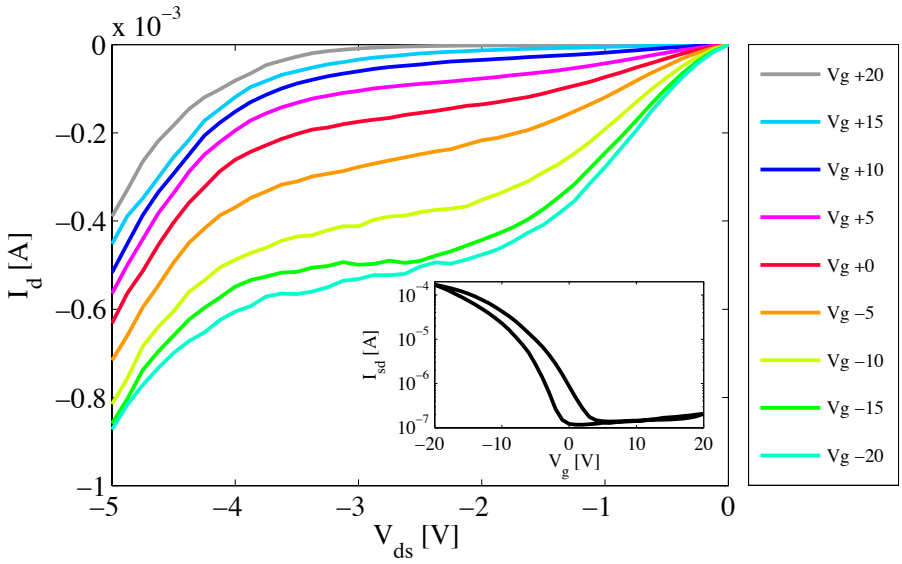

Figure 3.9: Output characteristics of nanowire SB-FETs with native oxide: Devices show unipolar p-type behavior. Inset shows transfer characteristics of the depicted device. With a back gate oxide thickness of 100 nm the device showed decent gate coupling and on/off ratio of 10^3. The output characteristics reveal a non-linear current increase at low V_{ds} typically for barrier determined transport. A saturation regime and subsequent break down follows at higher V_{ds}.

oxide device exhibits an output charteristic of a p-type MOSFET with non ohmic contacts. Figure 3.9 displays an exponential increase of I_{sd} with V_{ds} for low V_{ds} which is a common indicator for SB determined transport. It reflects the effective barrier reduction with LEF for both drain and source contact. A saturation region, where the channel potential is equal to the drain potential and the conductance declines, follows. In standard MOSFETs this is called pinch off region, here the saturation is less pronounced. A second region with nonlinear conductance increase occurs beyond $V_{ds} = -4$V. A possible reason might be avalanche effects [215, 216]. This is further supported by the fact that shortly after this avalanche regime device break down is immanent. Surpassing V_{ds} of -5 V leads to a gradual permanent degradation of currents. Indeed it can be observed, that the shape of the transfer characteristic is not changed but the overall I_{sd} are dropping in each transistor regime. High energy charge carriers in the channel can introduce deep trapped charge. Such fixed charges could lead to a constant turn off of surface orientated parts of the nanowire interface where the gate coupling is low. Also possible could be fixed trap charge generation due to high gate-drain or gate-source fields by gate oxide break down. Trapping might happen then especially close to the Schottky interfaces. Another explanation is the breakdown of individual devices in the nanowire array during electrical stress reducing the overall current in all transistor regimes. The different thermal expansion coefficients of Ni inter electrode and Si nanowire could probably lead to lost electrical connecting to the Ni inter electrode during device self heating for high V_{ds} due to mechanical stress.

3.4.2 Ambipolar output characteristics of nanowires with dry oxidized shell

The representation of output chararacterisitics of ambipolar devices is more difficult. Trends are similar for all back gated and top gated devices. The device presented here, is a top gate device with IE spacing of 10 μm composed of nanowires with thermally grown oxide shell. Back gate SiO_2 thickness is 400 nm, the Ni top gate has a 20 nm thick Al_2O_3 gate dielectric. The device underwent a 300^0C N_2 anneal for 10 min as discussed in previously. Transfer and output characteristics of the device are presented in figure3.10. The current is composed of n-and p-charge injection which are both affected by V_{ds}. Analogous to the IE spacing series, which showed the effect of LEF scaling on the transfer characteristics, one can observe an increase in off-current with increasing LEF. Off-currents increase more than on-currents. This arise again from a tunneling increase and effective Schottky barrier lowering for both p- and n-type carriers. However, the situation is different, since not only LEF scale but relative Fermi levels of source and drain are changed with V_{ds} as well. For the minimum (off) current V_g (Φ_{ch}) should have a value between source and drain voltage V_{ds} to come as close as possible to the flatband case at both interface simultaneously. Therefore, the off-current position shifts towards negative (positive) V_g values for negative (positive) V_{ds}. The shift of the off-current position with V_{ds} shows an opposite trend like for LEF scaling by IE spacing reduction.

For the representation of output characteristics, off-current position and value are modified by V_{ds} which leads to a complicated progression. N- and p-conduction cannot be separately displayed since the intersection point of p- and n-branch is moving with V_{ds}. I_{sd} is shown in dependence of V_{ds} for positive and negative V_g here. For both n- and p- conduction the SB related non-linear current increase at V_{ds}=0V and subsequent saturation regime is observed. The presumable avalanche effect appears only for high abs(V_{ds}) for the depicted device. This is likely to arise from the long SiNW channel length (3 μm) of the device for which avalanche supporting high LEF are only build up for very high V_{ds}.
Finally to note, the peak transconductance is increasing for all devices with V_{ds}, although the subthreshold slopes are decreasing.

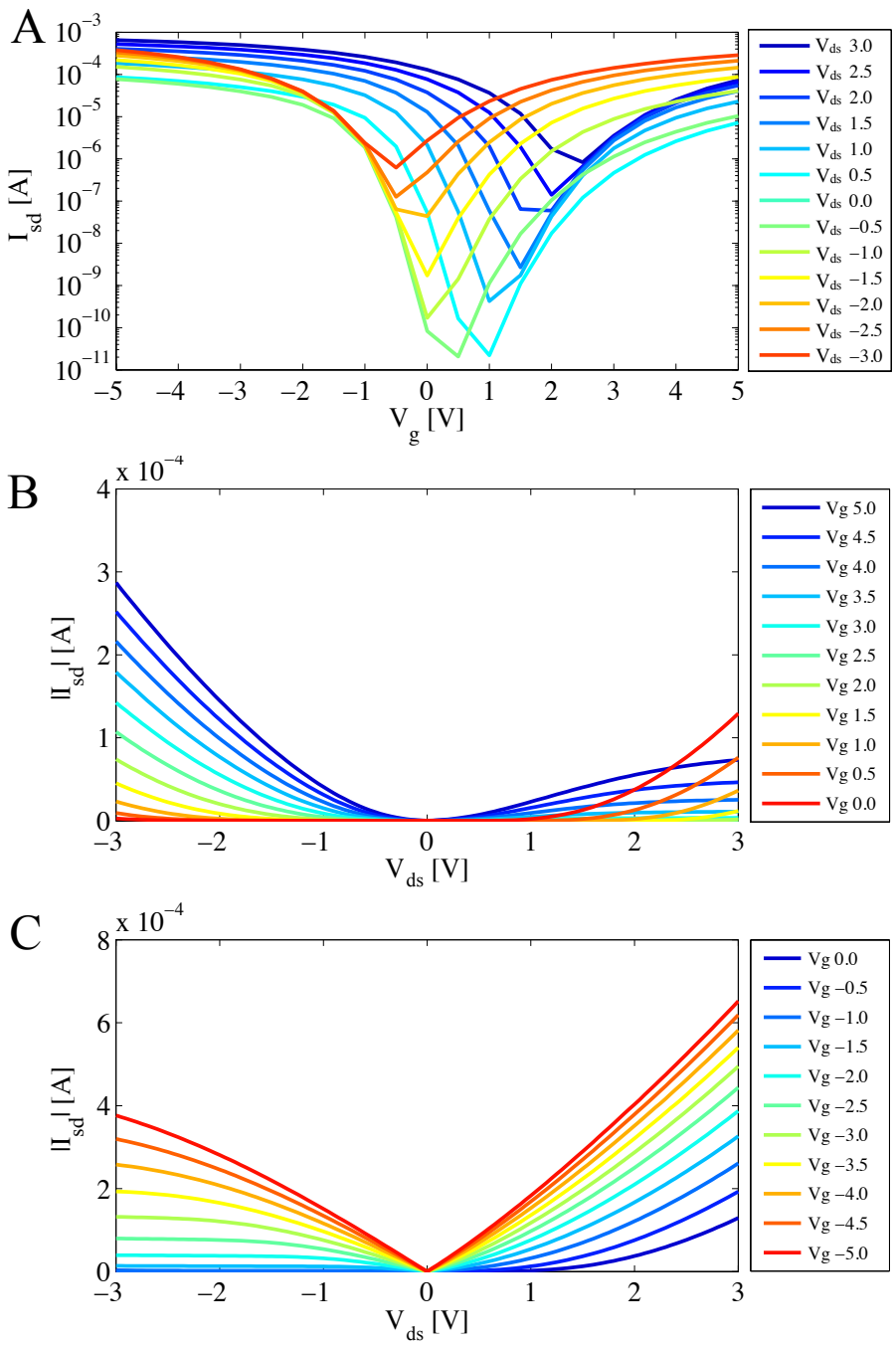

Figure 3.10: Source/drain voltage V_{ds} dependence of charge transport in thermally oxidized nanowire SB-FETs: A) Transfer characteristics show ambipolar behavior with non trivial dependency on V_{ds}. For large absolute value of V_{ds} the device cannot be turned off; p and n-type charge carriers are assumed to significantly contribute simultaneously to the conduction over a wide range around the minimum current. Since both p and n-currents are present at the same time for larger V_{ds}, the output characteristics cannot be separately drawn. Instead, output characteristics are depicted for B) positive and C) negative gate voltage here. Back gate SiO_2 thickness is 400 nm, Ni top gate has a 20 nm thick Al_2O_3 gate dielectric, IE spacing is 10 μm.

3.5 TEMPERATURE DEPENDENCE

Many important parameters of the transistor, like current levels, transconductance and subthreshold swing, are temperature dependent. Temperature drifts, for instance by self heating due to resistive losses, lead therefore to a gradual change of device parameters which results in false signals and varying sensitivity. This chapter shows the impact of temperature on the transistor. The measurements were performed under a nitrogen N_2 purge in a shielded probe station (Süss Microtec) with a temperature controlled chuck. Transfer functions were measured for 14 different temperatures ranging from 20 ^{0}C to 160 ^{0}C by adjusting the chuck temperature to the desired value. A plot of the transfer functions vs. the temperature T is depicted in figure 3.11. On and off-currents and subthreshold swings are replottet below for a better overview. With T, the on-currents increase ($\Delta I_{on} = 0.12\,mA$) and off-current increase up to several orders of magnitude ($\Delta I_{off} = 10\,nA$). The off-currents are measured in the subthreshold region where the current depends exponentially on T, as can be seen from equation 1.3. For higher T, in the subthreshold regime, more charge carriers have sufficient energies to overcome the energetic barrier via thermionic emission. The increase of on-current comes from the enhanced generation of charge carriers in the semiconductor but mainly from the modified Fermi distribution in the metal leading to a higher tunneling rate. Transconductance is increasing with T, because of higher currents in the tunneling regime. The subthreshold swing S is given by $S = 1/\kappa\ 59mV/dec\ T[K]/300$. These swings are depicted in figure 3.11B with assumed gate coupling factors $\kappa_p = 0.12$ and $\kappa_n = 0.08$. However, the subthreshold swings extracted from the measurement data show a more pronounced degradation with T than predicted by theory. The reason is an enhanced electrical hysteresis, which is also assumed to be a cause of strong off-current increase towards growing T, similar to the observations show in section 3.3. Indeed, extracting of device intrinsic parameters (like SB heights) via Arrhenius plots can not be performed since the information is covered by growing hysteresis amplitude with increasing T. The reasons could be higher probability of chemicial surface reactions, increased ion mobility or excess energy for charge carriers to tunnel into deep traps. The mobility of possible contaminant ions (Na, K) strongly increases for temperatures above 150 ^{0}C [217]. Additionally heating promotes a long time stable V_{FB} shift to more positive voltages which can be observed after reduction of the device temperature. For the sensor, the increased hysteresis poses a problem because more drifts are likely to occur disturbing the measurements. Especially for sensor operation in the subthreshold regime, the temperature has severe effect on the output currents.

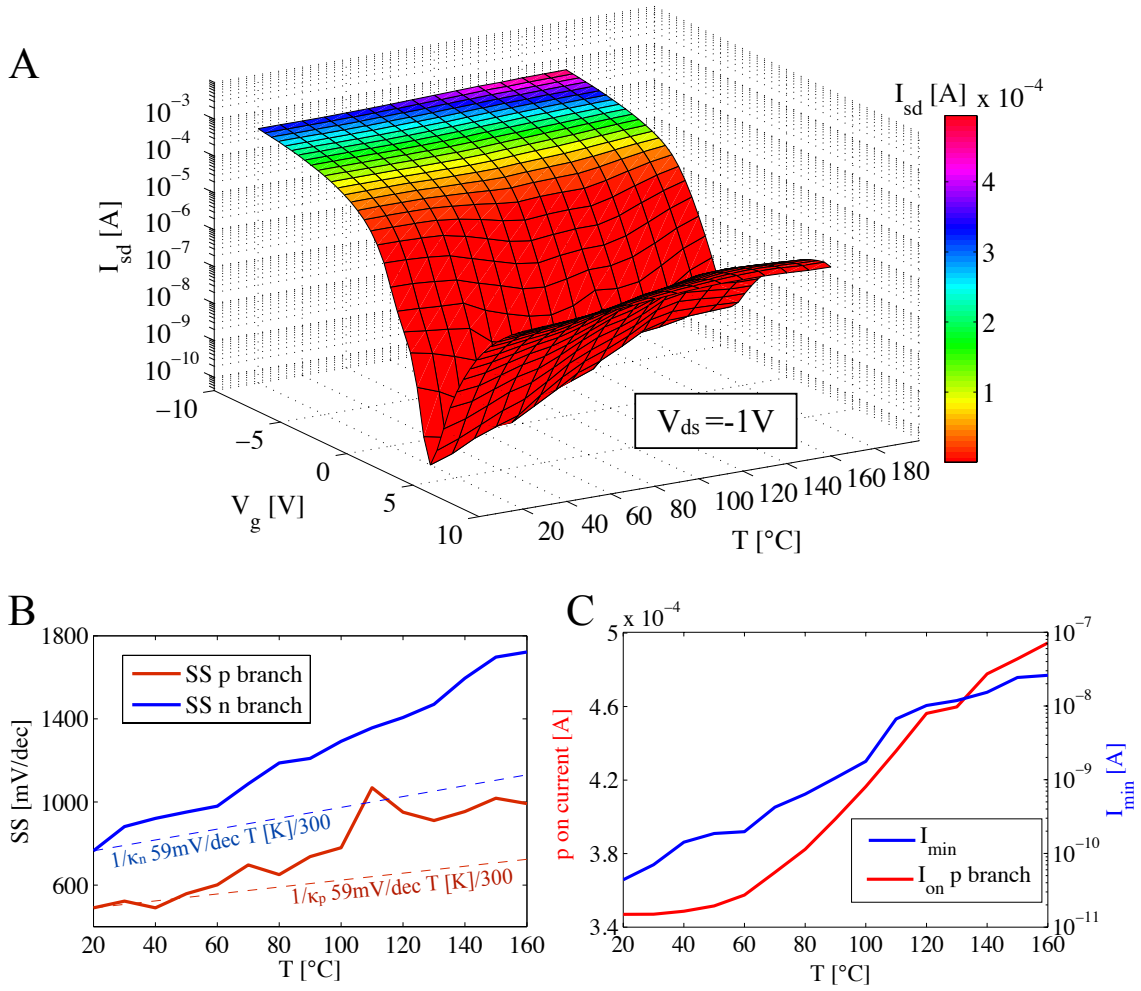

Figure 3.11: Transfer characteristic temperature (T) dependence of back gated nanowire device with thermally grown oxide shell: A) transfer characteristics vs. T at V_{ds}=-1V. B) Subthreshold swings are degraded with growing temperature. Degradation is stronger than predicted by theory (dashed lines), most probably due to a growing hysteresis and/or charge trapping with T. Gate coupling factors of $\kappa_p = 0.12$ and $\kappa_n = 0.08$ are assumed. C) On-currents are hardly affected around room temperature but increase approximately linearly above 60 ^{0}C, off (min) currents increase exponentially.

3.6 TRANSISTOR NOISE

Noise is determining the lower detection limit of the sensor. The transistor related noise is characterized here. Device noise is related to tunneling currents through Schottky junctions (Poisson or shot noise) as well as charge trapping and generation recombination (G/R) noise in the conduction channel. Additional noise is produced in the serial resistivities, e.g. the thin inter electrodes. As described in chapter 1.3.2 the power spectral density S_I can be expressed as:

$$S_I = \frac{I_{sd}^2 * \alpha}{f^{\beta} N} \tag{3.4}$$

Figure 3.12B shows the normalized frequency dependence of S_I/I_{sd}^2 for various V_g. Long and short channel parallel array devices with planar top gate were characterized. A long channel (IE spacing 10 μm, channel length approx. 7 μm) and a short channel (IE spacing 5 μm, channel length approx. 2 μm) device are shown in the graph. The channel resistance for the long channel devices is orders of magnitude higher than the lead resistance. The α parameter cannot be extracted since N is unknown. N, I_{sd} are affected by V_g, N additionally by the nanowire length. For small $|V_g|$, two distinct powers of the 1/f noise are observed. For the low frequency end this arises from the trapping related noise with $\beta \sim 1$. For higher frequencies, possibly G/R noise could be the source of the noise component with another 1/f power $\beta > 1$. For frequencies above 5 kHz the transistor noise level is already lower than the noise from the amplifier stage of the measurement system.

For small IE spacings the channel resistance becomes comparable to the lead resistance. For the short channel devices additional irregular noise components were found in the very low frequency end of S_I/I_{sd}^2. These noise components are not a multiple of the power line cycle (50 Hz). They show probably a high impact of the serial resistances to the noise characteristics. Noise is produced in the thin metallic electrodes and at the contact area of probe needle to electrical contact pad. Probe needles are mechanically pressed on the pad to ensure the electrical contact. For all measurements ever performed, the probe needle contact resistance was observed to vary strongly and unreproducibly with mechanical pressure. The pads are deformed by the needle, temperature increases at the contact area and can lead to thermal expansion. The exact total contact area is thus unknown and might also fluctuate by vibrations of the setup. The 10 Hz component of the normalized PSD S_I/I_{sd}^2 is depicted in figure3.12C. S_I/I_{sd}^2 decreases with I_{sd} like expected. However, for short channel devices S_I/I_{sd}^2 increases again for currents higher than 20 μA. This is a non typicial behavior of transistor noise. The pad-to-needle resistance R_c is assumed to be responsible for the irregular noise behavior at large V_g, when R_c is similar to the channel resistance.
For a qualitative estimation of the SNR and its dependence on the nanowire length, I_{sd} was measured with a fixed gain (Keithley measurements system) for various V_g. The exact value of SNR depends strongly on the measurement configuration. V_{ds} was fixed at -0.5V, current integration

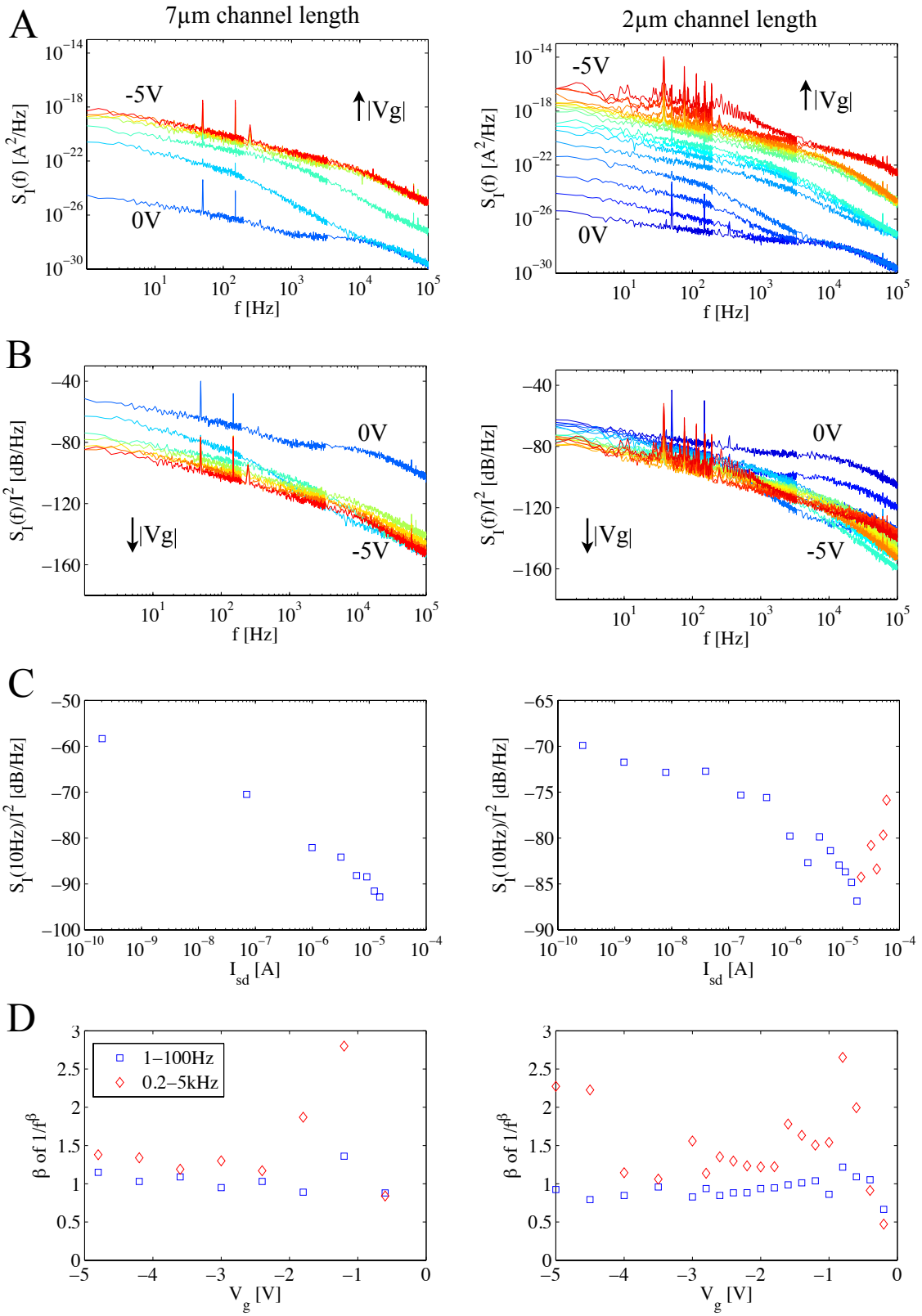

Figure 3.12: Power spectral density S_I of long and short channel nanowire SB-FETs. Gate voltage was swept from 0 to -5V (blue to red) to capture the noise characteristics over the whole p-branch slope. A) Frequency dependence of S_I. B) Normalized power spectral density S_I/I^2 in dB. C) 10Hz component of S_I/I^2 vs. source-drain current I_{sd}. S_I/I^2 is dropping towards larger I_{sd}, i.e. conduction channel charge Q_{ch}. For short channel devices with a high current output, S_I/I^2 increases again for high I_{sd} ($>20\,\mu$A) due to parasitic resistance related noise. D) Exponent β of 1/f noise at low and high frequencies.

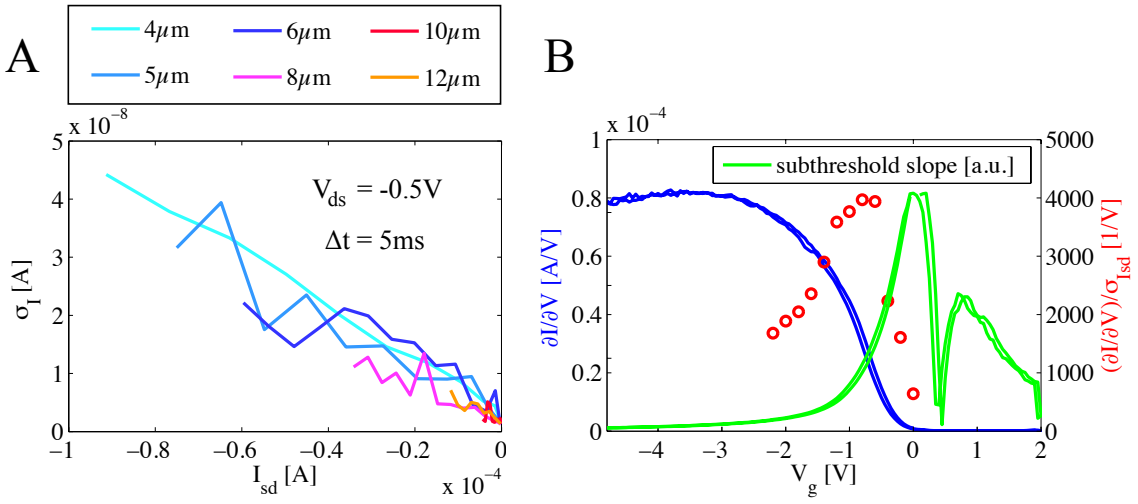

Figure 3.13: Current noise and signal to noise ratio (SNR) as a function of current: A) Current noise σ_I vs. current I_{sd} for various IE spacings. Approximate linear scaling of noise with current is observed for all devices. B) Transconductance $\partial I_{sd}/\partial V_g$ and $\partial I_{sd}/\partial V_g$ to noise σ_I ratio ($\sim$ SNR) vs. gate voltage V_g. Since current noise increases more than transconductance beyond -1V of V_g the SNR maximum is found between subthreshold regime and peak transconductance. The logarithmic slope $\partial \log(I_{sd})/\partial V_g$ is plottet in green to indicate the peak subthreshold slope.

time was fixed to 5 ms. From the recorded I_{sd} the rms value σ_I was calculated. For all IE spacings σ_I was observed to scale approximately proportional to I_{sd}. Transconductance and SNR/$\Delta\Phi$ are depicted as a function of V_g in figure 3.13. For the higher transconductance and lower charge trapping, only the p-branch is observed. The peak SNR appears after the subthreshold regime but before the peak transconductance. Indeed, this shows that the optimal working regime for the sensor is neither the subthreshold or the peak transconductance regime. The reason is the strong noise increase with I_{sd} and the peak transconductance shifted to high V_g (i.e. I_{sd}) because of the SB related resistance (see chapter 5.2.1). The larger α, the more the peak SNR is shifted towards the subthreshold regime. For a very low transistor noise level, the peak transconductance regime will be preferred for sensing.

It was observed that peak SNR value and position are independent of IE spacing, i.e. nanowire length. Although short channel nanowire devices show a higher transconductance they also show a higher noise level. The reason of the transconductance increase towards decreasing IE spacing is due to the increase in total current I_{sd} since κ is essentially independent of IE spacing for top gate devices. Since current noise σ_I and transconductance are both scaling proportional to I_{sd}, their ratio, i.e. SNR is essentially constant. To increase the SNR, the charge carrier density or κ should be increased while keeping the operation current I_{sd} constant.
Since a strong impact of the contact resistance was found, the noise at the peak transconductance could also be caused by serial resistance. The contact related noise can lead to the SNR diminish-

ment at higher I_{sd}. Note, that probably not transistor noise limits the SNR but the bad contact of probe needle to electrical contact pad. It is strongly suggested to decrease the lead resistance and the contact resistance by a proper chip bonding to fully exploit the low noise characteristics of silicon nanowires.

4 PH MEASUREMENTS

This chapter summarizes the results obtained from the measurements of the SB-FET pH sensor. The performance of three sensors with different IE spacing are compared. The IE spacing dependent trends of transconductance and subthreshold slope found in chapter 3 were found to be valid for liquid gated SB-FETs as well. In contrast to output current and the peak transconductance level, the mean SNR was found to be independent of the IE spacing.

4.1 EXPERIMENTAL SETUP AND DATA ANALYSIS METHOD

A millifluidic channel (dimensions 2 mm x 1 mm x 15 mm) made of polydimethylsiloxan (PDMS) is mechanically pressed on the measurement chip and was confirmed to be liquid leak-tight. Teflon capillary tubings are connected to inlet and outlet of the channel to deliver the electrolyte solution with specific pH. The fluid pH sample is suctioned from a reservoir with a automated syringe pump through the channel to a disposal containment. To both inlet and outlet tubings Ag/AgCl reference electrodes are connected. The use of dual reference electrodes was found to be essential to avoid severe electrostatic disturbances from the environment. PH solutions were made from phosphate buffer for pH 7 to 5 and acetate buffer for pH 4-3. The pH was controlled with a commercial glaselectrode pH meter. The error of pH by this measurement can not be estimated. The ionic concentration of the buffer solutions was 10 mM.

For biosensor experiments, operation in constant current mode is strongly recommended for the reasons given in chapter 1.3. Mainly for research purpose, a different electrical measurement method for the determination of the surface potential was chosen here. The liquid gate potential V_{lg} was swept during the sensing experiments to measure the full transfer characteristic over time. In this way the sensitivities for each transistor regime could be determined for the relevant sensing

experiment and compared to the data from top gate devices. In addition, the first chemical surface functionalization experiments showed an extreme change of n-conduction in particular (chapter3), other groups reported for SB-FETs like CNTs a modulation of the SB height and gate capacitance in sensing experiments [85, 218] and the double layer capacitance was reported to be pH dependent [219]. All these findings could lead to a change of slope and shape of the transfer characteristics whereas the ISFET theory and working principle demands a pure threshold voltage shift ΔV_{th} upon surface-analyte interaction. Therefore, it was necessary to investigate the transfer characteristics as a whole.

To obtain the transfer characteristics the liquid gate potential V_{lg} is swept from 2 V to -3 V (down sweep) in 40 steps and back from -3 V to 2 V (up sweep) in another 40 steps. In total there are 80 V_{lg} data points recorded for each transfer function. The source/drain current I_{sd} for each V_{lg} data point is recorded with a fixed current integration time of 0.05 s leading to a total sweep duration of 4 s. Sweeping of the back gate potential was done synchronously to the liquid electrode to decrease the probability of oxide breakdown. The first measured I_{sd}-V_{lg} curve is used as a reference curve. From the succeeding I_{sd}-V_{lg} data, ΔV_{th} can be calculated by comparing the actual I_{sd}-V_{lg} data pairs with the reference curve. In doing so, for each V_{lg} the same value of V_{th} are derived like they would be obtained from the constant current mode measurements.

4.2 TRANSFER FUNCTION IN ELECTROLYTE WITH LIQUID GATE

Figure 4.1 shows the transfer characteristics in electrolyte for two different pH values. Referring to chapter 3, one can see, that the gate coupling is comparable to the top gate device with the same front dielectric Al_2O_3 layer. Nevertheless the liquid gate coupling is lowered by the electrolyte double layer (ionic concentration dependent), introducing a serial capacitance. Interestingly, the transfer curves of the sensor devices are also not centered like for SiO_2 and Al_2O_3 covered back gated devices with floating surface potential. Since the curve is shifted to positive gate voltages for every pH value, the possibility of surface group charging is excluded as a possible reason.

4.3 SENSOR RESPONSE ON PH

In the following, the sensor response on pH and resulting surface potential changes is demonstrated. Using an Al_2O_3 ionsensitive layer, $\Delta V_{th}/\Delta$pH is expected to be independent of the pH value and be close to the Nernst limit 59 mV/pH [220–222]. Also pH response hystersis and sensitivity to alkali ions is smaller compared to SiO_2 since Al_2O_3 poses an ion diffusion barrier [178, 223, 224].

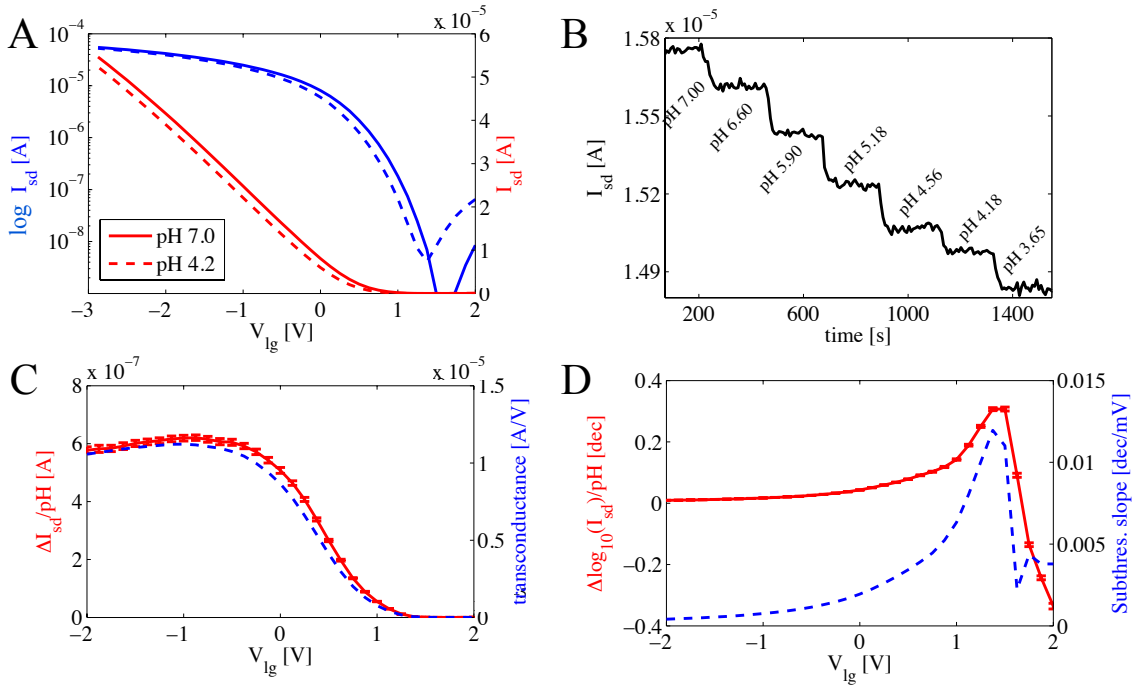

Figure 4.1: Transistor response of SB-FET parallel arrays (IE spacing = 8 μm) with Al_2O_3 ionsensitive oxide layer on pH changes. A) Transfer characteristics for two different pH values (pH 7.0, pH 4.2). Threshold voltage V_{th} shifts according to surface potential adaptation on pH change. An increase of off-current is observed as well, probably due to temperature drift during measurement. ΔV_{th} of 56 mV/pH is close to the Nernst limit (59 mV/dec). B) Recorded current modulation ΔI upon pH change. C) ΔI per pH is directly related to the transconductance at the corresponding liquid gate potential V_{lg}. D) The relative current modulation $\Delta\log(I)$ is proportional to the subthreshold slope.

The pH was changed in steps ΔpH over time and the threshold voltage shift per pH $\Delta V_{th}/\Delta$pH was derived. Solutions with defined pH were circulated through the millifluidic channel with a flow rate of 500 μl/min. Pumping stopped after 1 ml of solution was drawn from the reservoir and measurements continue in static conditions for 2 min before the next pH solution is pumped over the sensor interface. The pH was swept from pH 7 to pH 3.6 (down sweep) and again to pH 7 (up sweep) to investigate the hysteresis of the pH response.

Figure 4.2A shows the shifts of the transfer characteristic and transconductance for various pH obtained. It can be seen, that the shape of the transfer characteristics and transconductance is not changed. Only the threshold voltage is changed depending on pH in accordance with ISFET behavior. The pH response was measured for 3 devices with IE spacings of 6 μm, 8 μm 10 μm. As mentioned in section 3, for a pure V_{th} shift, the measured ΔI_{sd} at a given V_{lg} is proportional to the transconductance at this V_{lg}. The relative current modulation $\Delta I_{sd}/I_{sd}$ is highest in the subthreshold region and increases with the subthreshold slope. $\Delta I_{sd}/I_{sd}$ and ΔI_{sd} are plottet for the 3 devices and all V_{lg} in figure 4.2. The error bars and mean values are derived by 20 measured transfer characteristics (80 s measurement time) in steady no flow conditions. As was stated already

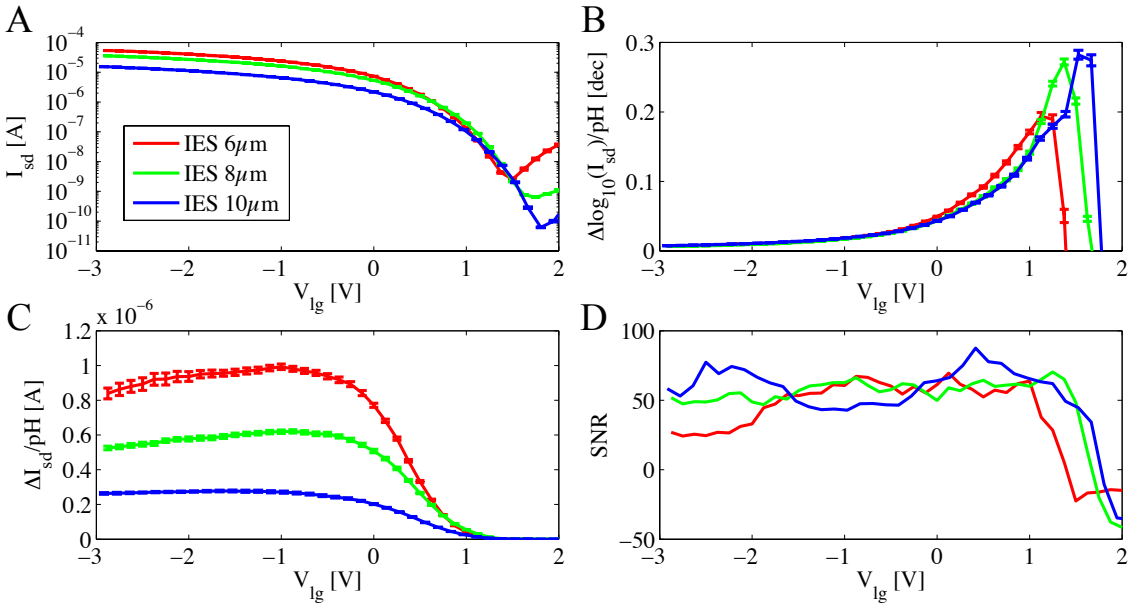

Figure 4.2: Sensor response and signal to noise ratio (SNR) in all transistor regimes for 3 different Si channel lengths: A) Transfer characteristics of sensor devices with 6, 8, 10 μm IE spacing with liquid gate. Short IE spacings exhibit highest current. B) Relative current modulation $\Delta\log(I_{sd})$ per pH. Slightly better gate coupling and thus steeper subthreshold slope of long IE spacing devices leads to higher $\Delta\log(I_{sd})/pH$. C) Absolute current modulation ΔI_{sd} per pH, which is proportional to the transconductance (not shown here). Highest ΔI_{sd} are achieved for short IE spacings.
D) SNR is essentially constant beyond the subthreshold regime ($V_{lg} < 1V$) and independent on IE spacing. It decays strongly in the subthreshold regime towards decreasing currents.

in chapter. 3, the transconductance increases for smaller IE spacings whereas the subthreshold slope decreases. This holds also true for liquid gated devices and is reflected in the sensor signals. Small IE spacing devices show high ΔI_{sd} but a smaller $\Delta I_{sd}/I_{sd}$.

For each V_{lg} the threshold shift was calculated by a comparison of the measured I_{sd} for the specific V_{lg} with the calibration curve taken at the beginning of the measurement. Note that only the p-branch is used for measurements. The calibration curve is therefore a monotonous function $V^0_{lg}(I_{sd})$. The threshold voltage shift ΔV_{th} at the time t is determined for each V_{lg} by subtracting the initial V^0_{lg} for the particular I_{sd}:

$$V_{lg} - V^0_{lg}(I_{sd}(V_{lg}, t)) = \Delta V_{th}(V_{lg}, t) \tag{4.1}$$

Figure 4.3A shows the mean value of the pH sensitivity $\partial V_{th}/\partial pH$ derived from a linear fit over all $\Delta V_{th}/\Delta pH$ for all measured pH values. As expected, the mean pH sensitivity is around 56 mV/dec independent on V_{lg}, i.e. the transistor operation regime [127]. There are small disparities for pH up and down sweeps and between different V_{lg} which could probably arise from V_{th} drifts and noise. Figure 4.3B shows the threshold voltage shift for the individual pH steps $\Delta V_{th}/\Delta pH$ at each pH for V_{lg}=-1V in the peak transconductance regime. For both pH up and down sweep the pH sensitivity is around 59 mV/dec but with strong deviations up to 20 mV/dec. These errors arise from noise but

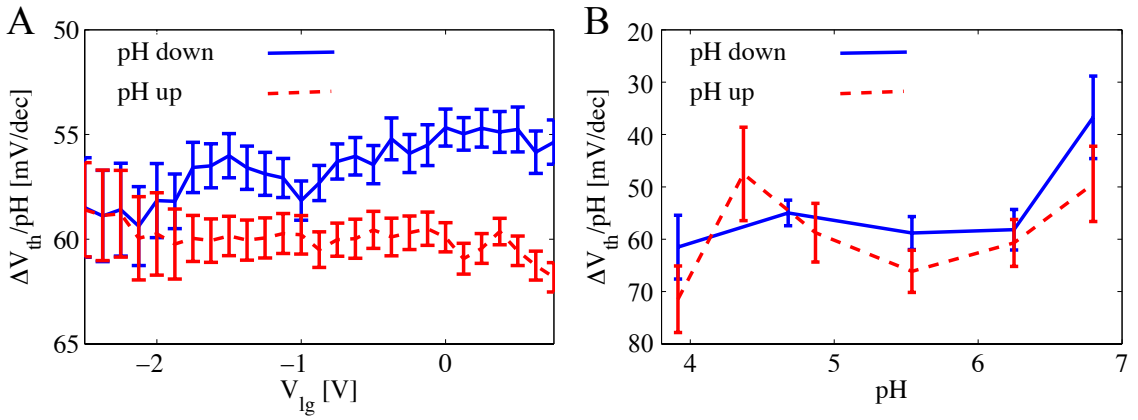

Figure 4.3: Extracted threshold voltage shifts ΔV_{th} on pH changes from pH sensor measurements: A) mean value of $\Delta V_{th}/pH$ over whole characterized pH range in dependence of applied V_{lg}. B) $\Delta V_{th}/pH$ for the individual pH steps at certain pH values. Measurements values are falsified by strong drifts and noise. In both graphics, the sweep to increasing pH (up) and decreasing pH (down) values is shown.

also to a large extend from drifts as discussed later. The standard deviation over 20 measurements is covered in the error bars. Additional deviations by drifts are not fully covered in the error bars and might be the reason for the observed deviations of ΔV_{th} between pH 7 and pH 3.6 (figure 4.3B). Indeed, noise from the electrolyte and V_{th} drifts are strong and might be the dominating noise source beyond the subthreshold region. The signal to noise ratio, defined here as mean value of $\Delta I_{sd}/\Delta pH$ to the standard deviation of I_{sd} over 20 measurements, is independent of the IE spacing and is essentially constant beyond the threshold voltage (figure 4.2D). In the subthreshold regime, the SNR decays strongly towards smaller currents. This indicates an insufficient current resolution from limitations by the transistor noise and measurements equipment. Therefore, the subthreshold region is not optimal as working regime of this type of transducer.

This finding is in agreement with experimental and theoretical results of many other groups [63–69]. It is contrary to the predictions from references [30, 71, 225], which propose to measure in the subthreshold regime because of the higher relative current modulation. Indeed, for CNTs it was found, that the maximum SNR is actually obtained when the device is operated in the subthreshold regime, since additional current noise arises in the on-state [70]. This feature, resulting in the need to operate the device at very low currents, makes CNT sensors vulnerable to external noise sources. Further, the shape of the transfer characteristics can be altered in biosensor experiments for CNTs, which was reported to result from modulation of the metal work function and thus Schottky barrier heights [85, 218]. Although the presented Si nanowire SB-FETs in this thesis exhibits exposed Schottky barriers, the transfer characteristics shape is not changed but V_{FB} (and thus V_{th}) is affected by the pH only. This behavior corresponds to the theory of ISFET based potentiometric pH sensors [48, 126].

4.4 SENSOR SIGNAL DRIFTS

Threshold voltage drifts are quite severe in the setup used and dependent on the ionic concentration of the electrolyte. Severe V_{th} drifts at low ionic concentrations (<10 mM) are the main reason why small surface potential changes can hardly be resolved using a single sensor element. When all terminal potentials are kept constant and I_{sd} is continuously recorded, V_{th} is stable for a continuous flow of the electrolyte solution. However, as soon as the flow stops, V_{th} drifts to more positive values and saturates at a level of a few 10 mV larger than the initial one. When the flow is turned on again, V_{th} returns to the initial level after the time τ. The time τ was found to be approximately the time needed for the solution to pass from the liquid electrode to the sensor interface. This was calculated from flow rate, millifluidic channel diameter and distance to reference electrode. Furthermore, V_{th} drifts were recorded in pulsed mode with 30 s pause interval in between the measurements during which all voltages were turned off. V_{th} drift were found to be minimal under this condition. Constantly applied terminal voltages are therefore shown to promote V_{th} drifts. Drifts could be caused by local heating of the sensor element and surrounding electrolyte at the surface due to resistive losses [226]. The temperature dependency was discussed in section 3. An increase of off-current was also observed during the measurement which could be an indicator for temperature drifts, i.e. device self heating. However, V_{th} drifts are observed to be additionally dependent on the ionic concentration here. With increasing ionic concentration the electrolyte resistivity is reduced. A charge redistribution in the electrolyte or current leakage through the Al_20_3 layer could cause V_{th} drift as well. An unknown capacitance is being charged when the potentials are disturbed externally. This capacitance could be the large source-to-drain inter electrode capacitance or the capacitance of millifluidic channel wall to sensor surface. The millifluidic channel walls have a substantial surface area with an undefined potential posing a large capacitance. When voltage is applied to the sensor, the capacitance between channel walls and sensor surface is being charged by displacement and leakage currents. The time scale for the drift is then given by the RC circuit, where R is the resistivity of the electrolyte. Therefore, long term drifts are observed for small ionic concentrations, corresponding to high R. When the electrolyte flow is turned on, the charge is rinsed away and V_{th} stabilizes again. The standard deviation of V_{th} was investigated as a function of ionic concentration in no-flow conditions. It was found, that after the drift correction by linear regression, the standard deviations, i.e. V_{th} noise, is the same for all investigated ionic concentrations (1 mM, 10 mM, 100 mM). However, drifts are extremely strong for low ionic concentrations.

5 SCHOTTKY JUNCTION IMPACT ON SENSITIVITY

In chapter 4 and 3 we pointed out the importance of the transconductance on the sensor response. The signal to noise (SNR) ratio is proportional to the transconductance to noise ratio. The Schottky barriers are a very important region of the SB-FET sensor since the charge injection and thus current modulation is mainly steered by band bending at the Schottky junction. For the most nanostructure SB-FETs (like CNTs), Schottky junctions are hidden under the source/drain electrodes which are additionally covered by a passivation layer to operate the device in electrolytes. Therefore, the Schottky junctions are covered and electrostatically weakly coupled to the electrolyte. The following experiments demonstrate the impact of the Schottky junctions on the transconductance. Two approaches are pursued and presented in this chapter. Schottky junctions are electrostatic decoupled from the liquid gate in pH solution which will show a decrease in transconductance. It will be shown, that the transconductance can be nevertheless overall increased by decreasing the Schottky barrier related serial resistance by the back gate.

5.1 SCHOTTKY JUNCTION ELECTROSTATIC DECOUPLING IN SOLUTION

The effect of electrostatic decoupling of Schottky junctions on the sensitvity $\partial I_{sd}/\partial pH$ is discussed in the following. As already shown in chapter 4, the sensitivity is given by the transconductance $\partial I_{sd}/\partial V_g$ x 57 mV/pH for an ideal Al_2O_3 front gate oxide. The transfer characteristics in solution show therefore all required information about the sensitivity. Schottky junctions and part of the

adjacent channel are covered by a SU8/Al_2O_3 stack. The gate coupling is locally lost or at least strongly reduced at the position of the Schottky junctions. This situation might be comparable to most alternative nanostructure devices with Schottky barriers, for which metallic contacts have to exhibit a passivation layer to operate in electrolytes.

5.1.1 Experimental setup in solution

A sensor chip was fabricated incorporating sensors with and without Schottky junction passivation. The chip has 5 working sensor devices with the same geometry which can be employed for pH measurements. The inter electrode (IE) spacing was chosen as 10 μm for the devices, the total silicidation length from both sides ($2l_{NiSi_x}$) was less than 8 μm but more than 6 μm. This was verified by evaluation of the transfer characteristics of the test structures on the chip. They showed the presence of fully silicidized nanowires for 6 μm IE spacing but fully semiconducting nanowires for IE spacings of 8 μm and larger. This leads to the conclusion, that for 10 μm IE spacing, the smallest channel lengths are likely to be larger than 2 μm. From the silicidation rate obtained in silicidation experiments a mean silicide length of 5 μm is expected for the applied annealing duration of 90 s. The silicide length distribution might be a bit broader than shown in the statistics from chapter 2.2.8 since the silicide mean value is longer. The chip was covered with 2 μm thick SU8 photo resist and windows were opened lithographically over the middle of the Si nanowire channel with 2 μm, 4 μm, 6 μm, 8 μm, 10 μm width for the 5 devices respectively. The chip was post annealed at 300 C in forming gas (H_2/N_2 1/20 p/p) for 30 min to densify the SU8. Since the Si nanowire channels are longer than 2 μm, one can state that for the device with 2 μm window width, all Schottky junctions are covered with SU8. After the SU8 structuring the whole device was covered with 20 nm Al_2O_3 by ALD. The SU8 is therefore sealed with the ion diffusion barrier Al_2O_3 which prevents electrolyte leakage under and in the SU8 [1]. Conclusively, the device with passivated Schottky junctions exhibits a 2 μm wide window in the protection SU8 layer, exposing the middle segment of the Si channel only. For the device with 10 μm wide window, Schottky junctions and Si channel are both exposed. The setup is shown in figure 5.1.

5.1.2 SU8/Al_2O_3 passivated junctions in electrolyte

Transfer characteristics of devices with passivated and exposed Schottky junctions (SJ) are recorded in ambient air with back gate and floating surface potential. Afterwards they were measured in pH 7 electrolyte solution (ionic concentration of 10 mM) via the liquid gate from the top surface while the source-back gate potential was kept constantly zero. The transfer characteristics and transconductance are depicted in figure 5.1.

[1] it was found to be a necessary layer since only covering with SU8 does not lead to a change of the transfer characteristics but to severe drifts and V_{th} instabilities

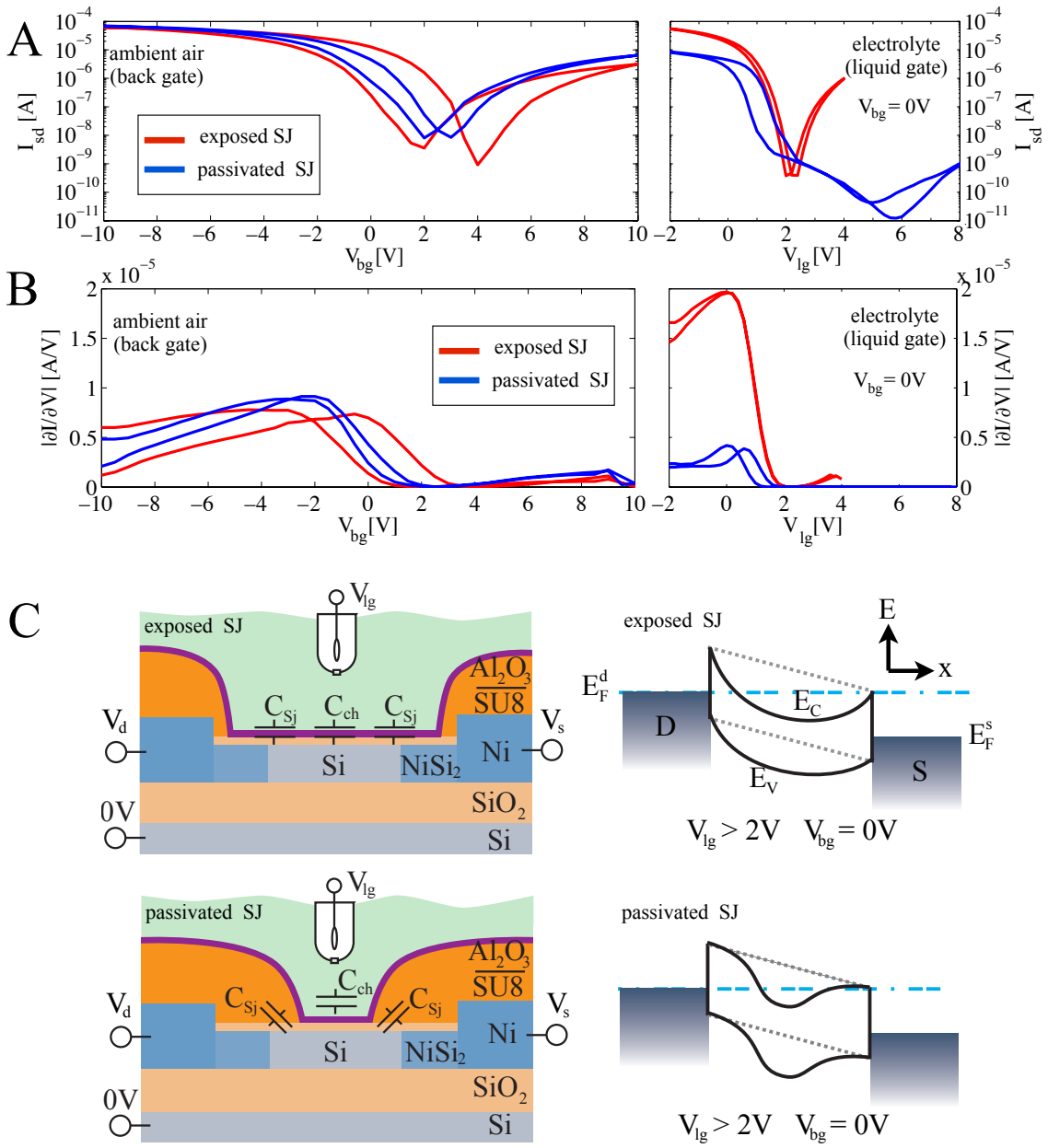

Figure 5.1: Effect of Schottky junction electric decoupling from electrolyte gate in SB-FET pH sensors: A) Transfer characteristics and B) transconductance for conventional pH-sensor device with exposed Schottky junctions (SJ) and a device passivated SJ covered by SU8 layer at $V_{ds} = -0.5$V. Electrical characteristics are recorded in ambient air with back gate and in electrolyte with liquid gate. The entire surface of both chips is covered by Al_2O_3 dielectric layer. Both devices show a better gate coupling in the subthreshold p-branch regime with electrolyte gate, resulting in a steeper subthreshold slope compared to the back gate characteristics. However, tunneling currents are strongly suppressed in the passivated SJ device. Apparently, the Schottky junctions are electrically decoupled from the electrolyte gate, and pose a constant high serial resistance. On-currents for p-type and transconductance are thus diminished. Since n-type carrier injection mechanism is mainly tunneling through the Schottky barrier, currents are suppressed efficiently and start to turn on only for very high positive V_{lg}. C) Schematic drawings of device cross section for passivated and exposed SJ combined with the expected energy band progression for positive V_{lg}.

For the dry state, both devices exhibit comparable subthreshold slope, on and off currents. The hysteresis of the device with passivated SJ and partly SU8 covered Si channel is reduced probably by a changed field distribution at the surface due to the additional dielectric layer or prevention of water adsorption. In electrolyte with gating from the top, the situation is totally different. The device with fully exposed Si nanowire channel, shows enhanced gate coupling and therefore a significantly increased transconductance compared to the dry state. Like discussed in chapter 4, the coupling increase arises from the thin top surface dielectric. For the device with passivated SJ, the transfer characteristics shape changed significantly. Most prominently, a strong suppression of n-conductivity is apparent. Only for high positive liquid gate potentials the n-conductivity increases slightly. The device turned quasi unipolar, also p-currents dropped by one order of magnitude. The transconductance is overall smaller compared to the back gate measurement in ambient air. However, the subthreshold slope has increased. This shows that not an overall gate coupling decrease by a thick dielectric layer is responsible for the change of the transfer characteristics. Indeed, to explain the higher subthreshold slope (better swing), the gate coupling to the middle segment of the Si nanowire channel has to be increased compared to the back gate device. It is assumed that a substantial portion of the subthreshold slope is dominated by thermionic emission[2] The schematic band diagram depicted in figure 5.1C visualizes the effect of local decoupling of the liquid gate by the passivation layer. In the subthreshold region, around the flatband case, the point of highest energy barrier is close to the middle of the Si nanowire channel. This point cuts off the thermionic emission of charge carriers. Therefore the middle segment of the Si nanowire channel modulates the charge injection in the subthreshold region. That is why the subthreshold slope is high for the passivated SJ device as well, although only the middle segment is exposed. It will be shown, that only a fraction of the nanowire channel has to have a good gate coupling to obtain a high subthreshold slope and on/off ratio, because the point of maximal potential energy determines the current level. For higher applied gate voltages, beyond the subthreshold region, the thermionic emission current is essentially constant (see chapter 1.2.6). The current modulation is significantly determined by the tunneling barrier thickness, which is controlled via the channel potential close to the $NiSi_2$-Si interface, i.e. the Schottky junction. Since for the passivated device this interface, and an essential part of the channel adjacent to it, is covered by the SU8/Al_2O_3 layer, the gate coupling is locally lost there. Gate fields cannot change the potential at the interface efficiently. Since the current is already relatively high in this regime, the peak transconductance is mostly determined by the ability to modulate tunneling currents. However, this ability is severely impaired due to the very low coupling at the Schottky junction, which is the reason for the intense diminishment of the transconductance. The Schottky barrier height is higher for n-type charge carriers ($\Phi_{Bn} > \Phi_{Bp}$). For the exponential dependence on this energy barrier, the thermionic emission is orders of magnitudes lower than for p-type currents. The dominant n-type transport mechanism

[2]Note that temperature dependent measurements could give additional evidence of these effects. However, such measurements were not technically possible during this thesis, given the liquid gate setup.

is tunneling. SB thinning and thus tunneling is suppressed efficiently by the Schottky junction decoupling and results in the vanishing of n-currents. Only for very positive V_{lg}, a slight Schottky barrier thickness modulation seems to be possible leading to a shallow n-current increase.
The implications for the sensor are clear. For the Schottky barrier based resistance being high for the whole V_{lg} range, the transconductance is overall diminished. Further, an increasing noise component coming from the higher SB resistance might be caused. Therefore the current modulation, i.e. sensor signals, are decreased and noise will probably increase additionally. This leads to an overall worsening of the SNR. To prevent loosing sensitivity, it is strongly recommend, for all types of FETs exhibiting Schottky barriers, to couple them well to the environment or eliminate the SB related resistance by other means. This can be done by biasing the back gate as will be shown in the next section. In contrast to other systems with passivated contacts, the nanowire system with intruded metallic contacts provides the possibility of exposing the Schottky contacts to the electrolyte.

5.2 MEANDER SHAPED GATES WITHOUT SCHOTTKY JUNCTION OVERLAP

The effect of exclusively gating the middle part of the silicon nanowire channel on the transfer characteristics was investigated. Devices are characterized in air. Inter digitated electrode devices were characterized with a meander shape top gate, only covering the inner parts of the nanowire channel. The Schottky junctions remained uncovered and were exposed to the ambient air. This leads to a back gate dominated potential at the Schottky junctions. A separate gate control of Schottky junctions and Si channel was therefore possible. By use of the back gate, the polarity of the transistor and Schottky barrier related serial resistance can be adjusted. The current modulation is in turn conducted by the meander gate through the channel only.
Further, a comparison of meander gate and planar top gate shows the effect of decoupling the Schottky junctions on transfer characteristics and transconductance. For a constant back gate voltage, meander gated devices were characterized. Afterwards the top gate geometry was changed for the same devices to a planar gate, followed by an electrical characterization. Planar gates cover all parts of the Si channel including Schottky junctions and source/drain contacts.
Meander shaped top gates (10 nm Ni + 20 nm Pt) were fabricated on interdigitated electrode devices with 4, 5, 6, 10, 12, 16 μm electrode spacings. The meander gates are 2 μm wide, the nanowire silicidation length is less than 2 μm from each side of the metallic contacts[3]. Nanowires have a thermally SiO_2 grown oxide shell. The entire surface is covered by a 20 nm Al_2O_3 dielectric layer, the back gate SiO_2 thickness is 400 nm. The setup is depicted in figure 5.2. For devices with

[3]All 4 μm IE spacing devices were operational. Most nanowires exhibit a shorter silicide segment length than 4 μm.

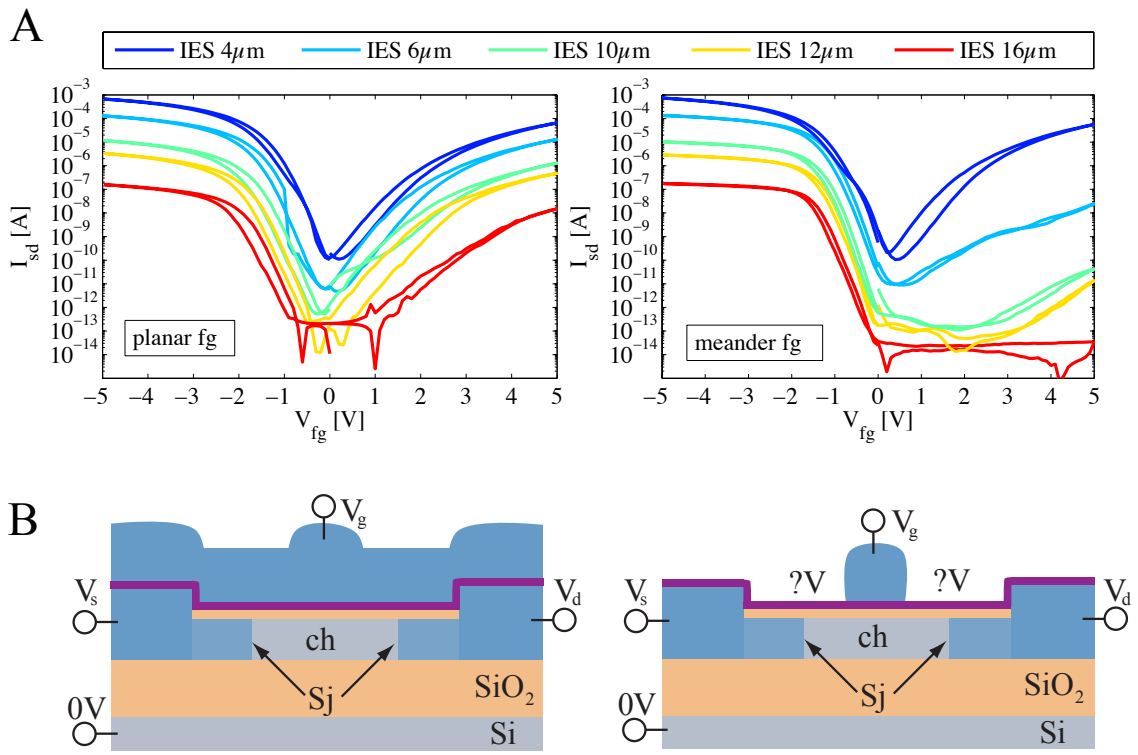

Figure 5.2: Impact of gradual loss of gate coupling at the location of Schottky junctions for SB-FETs in ambient air ($V_{ds} = -0.5$V): A) Transfer characteristics of devices with (right) planar top gates covering all transistors parts including Schottky junctions, (left) meander gate only covering the inner channel segment. B) Schematic drawings of device cross sections. Meander gate width is 2 μm for all inter electrode spacings (IES). For devices with IES of 4 μm Schottky junctions are covered as well. For larger IES, Schottky junctions are exposed to the ambient air.

IE spacings larger than 6 μm statistically no single Schottky junction is covered by the meander shape gate. Instead, the Schottky junctions are exposed to ambient air which was additionally confirmed by SEM investigations. As the spacings increase, the meander gate loses its impact on the Schottky junction part of the nanowire SB-FET. The back gate has a higher coupling to the Schottky junctions than the meander top gate in this case. Band bending at source and drain is dominated by the back gate and built-in potentials then. The Al_2O_3 surface over the Schottky junctions is facing the ambient air with a low dielectric constant. The channel potential under the meander shape gate is dominated by the front (meander) gate and almost not by the back gate. The reason is the thick back gate oxide, thin front gate oxide and omega front gate geometry, which lead to a high ratio of front to back gate capacitance.

5.2.1 Separated gating of Schottky junctions and channel

By separate gating of Schottky junctions and Si channel, the peak transconductance and polarity can be adjusted. This is demonstrated here for a device with IE spacing of 16 μm. The distance

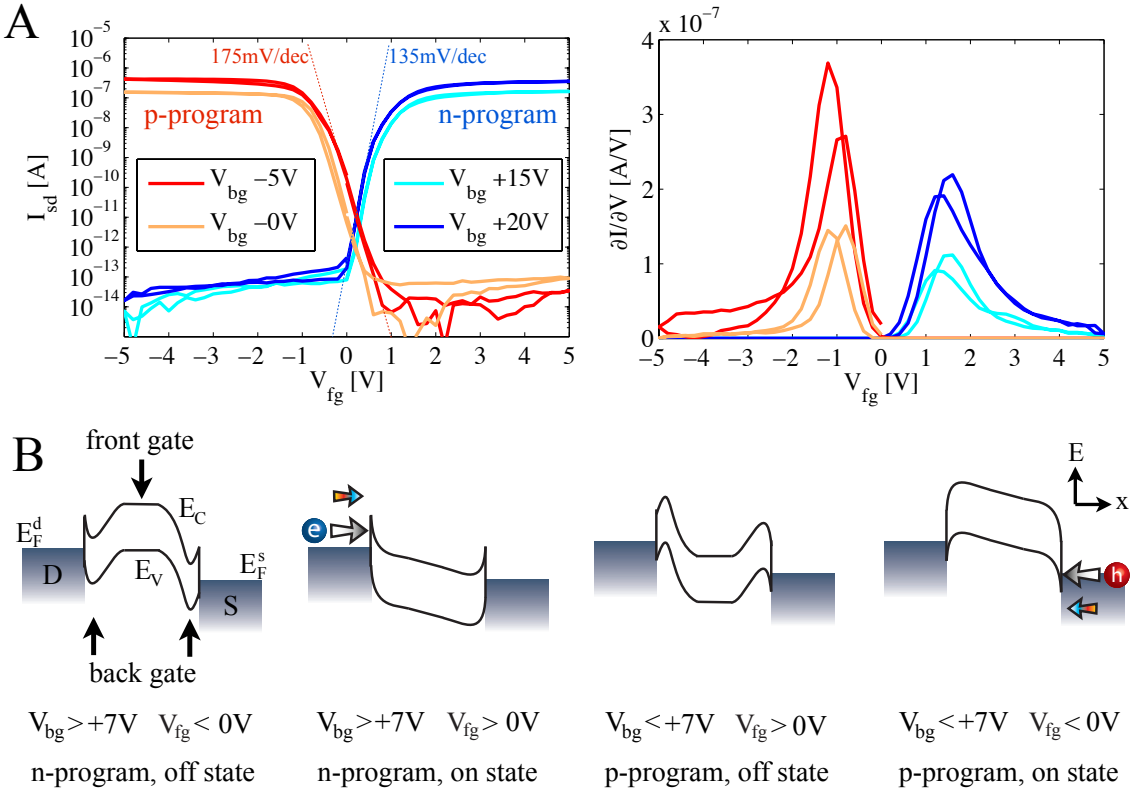

Figure 5.3: Reconfigurable transistor with adjustable polarity ($V_{ds} = -0.5V$): A) Transfer characteristics and transconductance for various back gate voltages V_{bg} controlling the polarity. B) Schematic energy band progression for various configurations. Middle segment of the channel and Schottky junctions are individually controlled via terminal voltages of a meander shaped front gate V_{fg} and the back gate V_{bg} respectively. By adjusting the Schottky barrier height and thickness by the back gate voltage V_{bg}, the resistance of both junctions can be minimized for either one of the charge carrier types. Hereby, the associated junction resistance for the other charge carrier type is maximized, leading to unipolar rectifying behavior in turn. The channel resistance and therefore entire current modulation is controlled via V_{fg}.

of Schottky junctions to the front gate controlled channel part is approximately 5 μm. Figure 5.3 shows the transfer characteristics I_{sd} vs. V_{fg} for different back gate voltages V_{bg}. The front gate is the meander gate with the terminal voltage V_{fg}. For V_{bg}=+15V and +20V the energy bands at the contacts are bent downwards. The junction resistance is highly decreased for electrons (n) but strongly increased for holes (p). Hole current is practically turned off (lower than measurement resolution), n-currents can be controlled with the front gate. The reason is, that the channel potential under the meander gate can be controlled separately, creating an additional energy barrier in the middle of the channel. Depending on the front gate voltage V_{fg} this energy barrier can be adjusted for n-currents. With this mid energy barrier the complete n-current can be controlled from the off to the on-state. The on n-current is determined by the Schottky junction resistance which is in turn controlled by the back gate only. If V_{bg} is changed to negative voltages the band bending direction is inverted at the Schottky contacts and the devices turns into a p-type device. Such a device is called reconfigurable transistor since the polarity can be adjusted by the external voltage

of a so called program gate (here the back gate). These devices have been demonstrated before this work, either in back and top gate configuration or by two separated top gates [11, 21, 81–83, 125, 227, 228]. However, this particular device shows a p-type transfer characteristics already for V_{bg}=0V. This is nevertheless simply explained by the flatband voltages V_{FB} of the individual transitor parts. Indeed, this device is a normally off (I_{min} at $V_{tg} = 0$), normally p-type (p-program at $V_{bg} = 0$) device. The normally p-type device behavior can be explained by the flatband voltage V_{FB} at the Schottky junction part of the transistor. V_{FB} is positive here, like for all back gated devices with missing top gate, due to uncompensated negative oxide charge previously shown in section 3.2.3. Positive V_{FB} means, energy bands are bent upwards for V_{bg} = 0V. A normally off behavior means, that the transistor is in the off state for a front gate voltage V_{fg}=0V. This results from a V_{FB} close to zero, like was demonstrated for non annealed top gate devices which are normally off as well. By adjusting V_{bg} the Schottky barrier thickness and therefore tunneling probability are regulated which determines the transistor resistance for the on-state. By increasing V_{bg} from +15V to +20V, the n-type on-current and transconductance are increasing. This shows that the transconductance of the transducer is limited by the Schottky barrier serial resistance in the first place. In the next section it will be demonstrated that individual gating of channel and Schottky contacts improves the transistor performance.

5.2.2 Enhanced transducer performance by reduced Schottky junction resistance

The transducer performance is compared for nanowire parallel array devices in two types of gate configurations. Devices with meander shaped top gates and IE spacings ranging from 4 to 16 μm are firstly electrically characterized. Meander top gate transfer characteristics are measured with source-back gate potential kept at V_{bg} = 0V. After the measurement, planar top gates are fabricated on top of the same devices covering all the nanowire channel including Schottky contacts for all IE spacings. The transfer characteristics are measured under the same conditions again. Transfer characteristics for both top gate geometries are depicted in figure 5.2. For smaller spacings the difference is not very pronounced. Especially for 4 μm IE spacing no change is observed. This seems reasonable since most or all Schottky junctions are already covered by the meander shaped top gate. The additionally processed planar top gate does not change the gate effectiveness. As the spacings increase, the meander gate does not cover the Schottky junctions and loses its impact on the Schottky barrier. N-type currents drop continuously compared to the overall gated device with planar top gates. P-type on-currents are remaining identical for meander and top gate devices for all IE spacings.

Figure 5.4 shows the comparison of meander and planar top gate for the device with the largest IE spacing of 16 μm. The n-branch currents and transconductance vanishes completely for the meander gate. The p-type on-currents and shape of the subthreshold region remain constant nev-

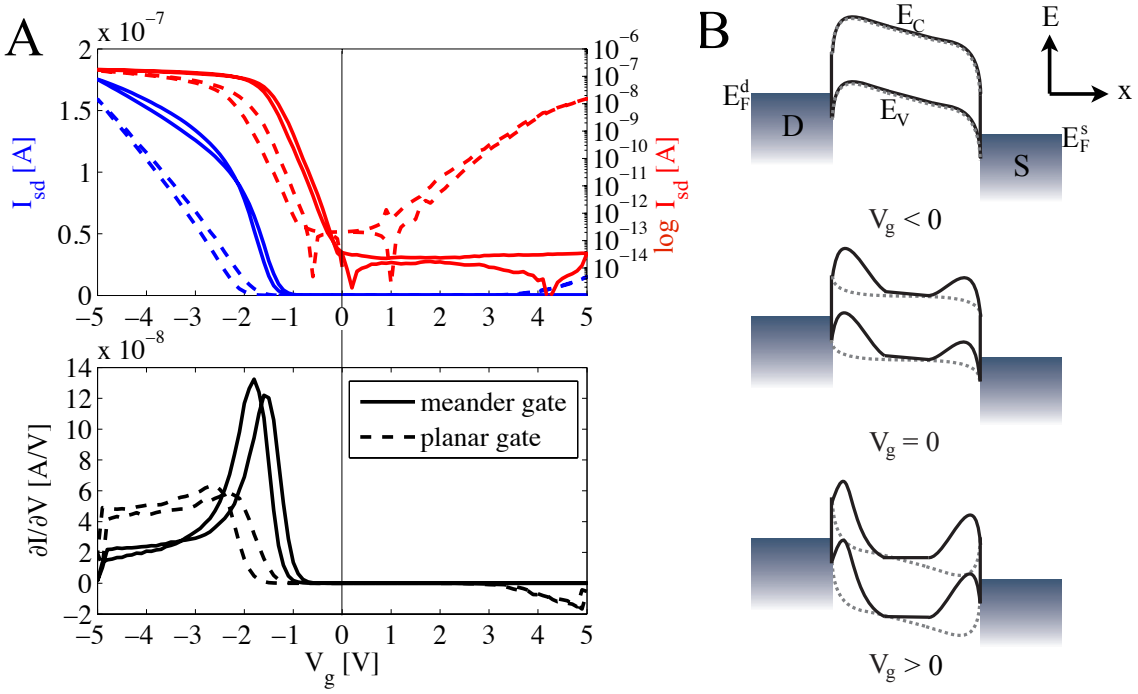

Figure 5.4: Impact of Schottky junction resistance on transducer capability ($V_{ds} = -0.5V$): A) Transfer characteristics and transconductance of 16 μm IE spacing devices with meander and planar top gate geometry. Meander shaped top gate only affects the middle 2 μm long segment of the Si nanowire channels. Schottky junction resistance is permanently lowered for p-conduction for given V_{FB} and V_{bg}. A high transconductance is observed compared to the standard planar gate device with high Schottky junction related resistance. B) Schematic band bending situation for both devices. For planar top gate devices (grey dottet line), the electric potential inside channel is controlled by the top gate in every part of the Si channel. For meander shaped gates (black solid line), only inner parts of the Si conduction channel are controlled. The Schottky junctions are dominated by built-in negative oxide charge, locally bending the Si energy bands constantly upwards.

ertheless. Unipolar p-type transistors are created in this manner, like described in the previous section. The energy band bending situation is schematically shown in figure 5.4B for meander (black solid line) and planar (grey dashed line) gate.

For meander gates and $V_{bg} = 0V$ the bands at the Schottky junctions are bent upwards in every transistor regime (for every V_{fg}). This constantly turns on the transmission capability for p-tunneling currents at the junctions. N-currents are suppressed at the Schottky junctions in every transistor regime independently of V_{fg} since the tunneling barrier is too thick and too high. The p-type on-currents of meander and top gate are similar for $V_{bg} = 0V$ due to the high positive value of the flatband voltage over the Schottky junction part. The transfer characteristics of the planar gate devices are hardly affected by the back gate voltage V_{bg}. For negative V_{bg}, p-type on-currents are higher, for positive V_{bg} p-currents are lower for the meander gate compared to the planar device. At the chosen $V_{bg} = 0V$, band bending is similar for both gates in the p-branch on-state.

Since p-type on-currents of both devices are similar at $V_{bg} = 0V$, the peak transconductance values can be compared to determine the transducer performance. From figure 5.4 one can see in the linear scale of the transfer characteristics that two linear slopes are formed for meander shaped top gates, whereas for planar top gates the slope is essentially constant after surpassing the subthreshold region. The peak transconductance in the p-branch highly increases for the meander shape gate. Further, the peak transconductance position is moved towards the subthreshold region and decays more rapidly towards the transistors on-state. Indeed, the middle energy barrier under the front gate is capable of turning the p-currents off completely and with a steep slope as the subthreshold regime is approached. Therefore, we see the total p-type current modulation happening within the subthreshold region by suppression of thermionic emission. The small ΔV_{fg} needed to switch from off to on-state leads to a high transconductance. For the planar gate, energy bands at the junctions are not pre-bent since $V_{FB} \sim 0V$. The Schottky junction related resistance for p-carriers has to be lowered by V_{fg} first to achieve the same output (on) p-current than the meander gate device. However, large V_{fg} are needed to bent the energy bands at the junctions efficiently. Therefore, a larger ΔV_{fg} is needed to switch from off to on-state, where the junction resistance is comparable to the meander gate device. Consequently, the transconductance is smaller. This result shows that it is not beneficial to introduce Schottky barriers in a transducer which need large gate terminal voltages to be levelled. However, the meander gate device showed that it is possible to reduce the Schottky barriers by separate gating. When current modulation is conducted by thermionic emission only, the transconductance is greatly increased. The subthreshold slopes and therefore gate coupling are identical for meander and planar shaped top gate. This shows that only a fraction of the conduction channel is needed to efficiently modulate the current. For a high enough band bending, the Schottky junctions might be almost transparent for holes. Then the maximum transconductance would be expected.

In contrast to the presented meander gate devices, the device measured in liquid in the previous chapter has a different V_{FB} over the Schottky junction part. This different V_{FB} arises due to the SU8/Al_2O_3 coverage and different coupling to the liquid electrode potential and increased the p-type tunneling resistance. The gate coupling is locally strongly reduced at the junctions which impairs the capability to tune the Schottky barrier resistance. Therefore, transconductance decreased significantly. However, for such devices the Schottky barrier could have been tuned by the back gate accompanying a notably transconductance increase. Current modulation can then happen by only exposing parts of the nanowire channel. Indeed, the back gate potential can be used for all kinds of CHEMFET sensors (on insulator) to tune the sensitivity which was shown by other groups [229–231].

6 SUMMARY AND OUTLOOK

During this work an innovative platform based on parallel arrays of silicon nanowire SB-FETs was developed and characterized. Nanowire growth was performed with synthesized Au particles leading to an uniform nanowire diameter distribution. Parallel aligned layers of nanowires were created via a printing process and contacted to Ni interdigitated electrodes by lithographic methods. After silicidation, axially intruded $NiSi_2$ phases are formed, generating a defined and sharp interface, a prerequisite to obtain homogeneous Schottky barrier (SB) heights. The entire chip surface is covered by an Al_2O_3 pH sensitive layer which also poses an electrochemical passivation.

Due to the large amount of nanowires in the array, the fabrication process yield is close to hundred percent and device-to-device variations are very low, especially for top gated devices. Parallel arrays of top down [232], superlattice nanowire pattern transfer (SNAP) [233] and bottom-up [94] nanowires were also reported from other groups and proposed for sensing applications. The fabrication scheme presented in this work is superior in terms of device-to-device uniformity of on/off ratio compared to the SNAP and bottom-up devices from references [94, 233].

Devices were fabricated with various inter electrode (IE) spacings. A statistical analysis of the transfer characteristics revealed scaling of on/off current, transconductance and subthreshold swing with IE spacing. Trends in the subthreshold regime, i.e. swing and off-current, are governed by the ambipolarity of the device and were found to depend strongly on the processing parameters. On/off ratios of over 10^8 and subthreshold swings of 120 mV/dec in the p-branch and 280 mV/dec in the n-branch are observed for the presented long channel (10-12 μm) nanowire SB-FETs. However, these parameters degrade gradually when scaling down the channel size.

The output currents are sufficient to apply the presented SB-FETs as driving stages for organic light emitting diodes or as transducers with stable outputs for biosensors. On-current of up to 400 μA per mm of electrode width are comparable to values for state of the art carbon nanotube (CNT) parallel arrays [234, 235] and organic thin film transistors [236] but lower than conventional

Si based MOSFETs. However, the potential of this technology is not yet fully exhausted. Nanowire separation is high in the presented devices. By closer packing of bottom-up grown nanowires reaching higher densities, e.g. via multiple prints, the output current can be significantly increased. The statistical data suggests that placing all nanowires in our device in direct proximity would result in an on-current density of about 25 μA/μm at V_{ds} = -0.5 V, which resembles state of the art thin film SB MOSFETs with dopant segregation [175, 237] and etched p-type nanowire parallel arrays [233]. The high current densities are a result of electrical field enhancement effect at the nano-sized tip of the intruded metallic $NiSi_2$ contacts, which strongly decrease the tunneling barrier width.
Although the current densities of undoped nanowire SB-FETs are significantly lower than complementary metal oxide semiconductor (CMOS) devices (1 mA/μm), they can be employed for reconfigurable electronics with enhanced functionality and can be printed on arbitrary substrates. This poses the possibility to transfer monocrystalline Si devices which underwent high temperature processes on flexible polymer foils.
Reconfigurable transistors can be produced with the SB-FET parallel arrays as demonstrated in chapter 5.2.1. Via a second gate, the transistor polarity can be inverted from unipolar p- to n-type. Therefore, the foundations to build a flexible complementary and thus power saving circuit platform on plastic substrates is laid down here. Steep subthreshold swings of 175 mV/dec for the p- and 135 mV/dec for the n-branch can be achieved, a great improvement to the single gate devices, especially for the n-branch. In contrast to single gated SB-FET, where the SB related tunnel resistance has to be additionally lowered, the slope remains steep until current saturation. By parallel assembly, the saturation currents can be enlarged compared to single nanowire reprogrammable devices [11, 21, 83, 227, 228]. Although the presented channel length of several micrometers are 10-20 times larger, on-currents are comparable with state of the art vertically stacked SB-FET parallel arrays [82]. So far, complex interconnection to produce multiple logic gates have not been demonstrated with reconfigurable devices. The high fabrication yield close to hundred percent for the presented nanowire arrays at a device density of more than 400/cm^2 can easily enable logic circuit fabrication by interconnection of individual transistors. Although the program gate was demonstrated with the back gate here, the process can be easily adapted for a top gate architecture. A predominant negative charge trapping was observed though, which is especially pronounced for natively grown nanowire Si oxide shells. This asymmetry poses a hindrance for the use of reconfigurable electronics, which demands symmetric branches of conduction.

To evaluate the feasibility of nanowire SB-FETs as transducers, the transconductance to current noise ratio, which is equivalent to the signal to noise ratio (SNR) [63], was investigated. It was shown that this ratio is not optimal at the peak transconductance regime. This is similar to other nanowire transistors and carbon nanotubes [69, 70]. The transconductance and absolute current modulation ΔI_{sd}/pH are decreasing with larger nanowire length, at the same time the relative

current modulation $(\Delta I_{sd}/I_0)/pH$ is increasing though due to steeper subthreshold slopes. This observation was also reported elsewhere for nanowire SB-FETs [238]. For the presented system, the regime for optimal transconductance to noise ratio was found at gate voltages significantly larger than the threshold voltage but before the peak transconductance. The reason is the steady increase of noise with source/drain current and a SB-caused shifted peak transconductance towards higher gate voltages, where source/drain currents and thus noise are already large. This is not essentially a result of a larger trap density of bottom-up grown structures compared to conventional FETs. Even planar MOSFET based ISFETs show this behavior which indicates that the SNR can be generally limited by the transistor noise at large source/drain currents in the first place [66]. The pH sensing experiment showed a SNR which is essentially constant after surpassing the threshold voltage. This indicates that the fluctuations of the surface potential, drifts and probably a chemically unstable Al_2O_3 layer were the dominating noise sources in electrolyte beyond the subthreshold regime. Indeed, the SNR in the subthreshold regime is decreasing continuously towards smaller transistor currents. Obviously, for very low currents and therefore low transconductance, the transistor current noise will limit the SNR. Because of the diminished current resolution, the subthreshold region is unsuitable as working regime of this transducer. Note, that the derived prediction of the SNR will only be valid if the half-cell potential can be homogenously created and the surface charge density is sufficient.

For SB-FETs, the peak transconductance scales proportional to the transistor current and appears at the beginning of the linear regime, where the SB are already thinned down strongly. Indeed, every serial resistance (also electrodes) reduces the transconductance and can even contribute significantly to the device noise as was demonstrated in chapter 3.6. The Schottky barrier represents a high serial resistance which is only lowered significantly far beyond the threshold voltage. As a simple transducer for a constant homogeneous surface potential, SB-FETs seem thus not to be optimal. However, by an adequate gate architecture, the negative influence of the Schottky barriers can be reduced. Chapter 5.2.2 clearly shows the impact of a local decoupling of the Schottky junctions from the electrolyte gate for a fixed high SB resistance. The transconductance was severely impaired. However, the SB related resistance can be strongly reduced by the back gate for the same device. This was demonstrated in chapter 5.2.1 showing a comparison of the transducing capabilities between a reconfigurable SB-FET with fixed but low serial resistance and a conventional SB-FET. The reconfigurable FET was created with a gate architecture, enabling a separate gating of Schottky junctions and Si channel. The Schottky barriers can then be permanently thinned down via the back gate (and built-in charge) which constantly reduces the SB related resistance. This device modulates the current in the middle segment of the nanowire only. Due to a constantly low SB related serial resistance the transconductance is very high compared to the SB-FET. At the threshold voltage, where the reconfigurable device transits to the linear regime, the conventional SB-FET still exhibits a high serial resistance due to a thick tunneling barrier. For the SB-FET, this barrier has to be thinned down additionally by going towards higher gate voltages. So the

Schottky barrier resistance hinders the increase of the current beyond the subthreshold regime. The peak transconductance is shifted towards larger gate voltages and is overall reduced compared to reconfigurable device.

This finding is of uttermost importance for other nano sensor devices with Schottky barriers like CNTs, ZnO [51], In_2O_3 [52] and others. For a given current and thus noise level, the transconductance and therefore transducer performance can be significantly increased by Schottky junction decoupling and appropriate back gate biasing. Also other groups reported the possibility to increase sensitivity by tuning electric device properties, including contact resistance, via the back gate potential [70, 229–231, 239].

The presented platform of nanowire parallel array SB-FETs can be employed to build up demonstrators for reconfigurable, complementary and power saving logic circuits, including the possibility to produce on flexible substrates. CMOS and doped nanowires with low Schottky barrier contacts show higher currents and therefore transconductance than the presented undoped SB-FETs. Nevertheless, since the noise scales with the current too, the transconductance to noise ratio are expected to be comparable. Therefore, and for the fact that the Schottky barrier related resistance can be additionally lowered by an adequate gate architecture, the applicability of the presented platform as transducer for future biosensor applications should not be excluded.

LIST OF PUBLICATIONS

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- Sebastian Pregl, Walter M Weber, Daijiro Nozaki, Jens Kunstmann, Larysa Baraban, Joerg Opitz, Thomas Mikolajick, and Gianaurelio Cuniberti. "Parallel arrays of Schottky barrier nanowire field effect transistors: Nanoscopic effects for macroscopic current output". In: Nano Research 6.6 (2013), pp. 381-388.
- Felix M Zörgiebel, Sebastian Pregl, Lotta Römhildt, Jörg Opitz, W Weber, T Mikolajick, Larysa Baraban, and Gianaurelio Cuniberti. "Schottky barrier-based silicon nanowire pH sensor with live sensitivity control". In: Nano Research 7.2 (2014), pp. 263-271.
- Thomas Mikolajick, Andre Heinzig, Jens Trommer, Sebastian Pregl, Matthias Grube, Gianaurelio Cuniberti, and Walter M Weber. "Silicon nanowires - a versatile technology platform". In: physica status solidi (RRL)-Rapid Research Letters 7.10 (2013), pp. 793-799.
- Daijiro Nozaki, Jens Kunstmann, Felix Zörgiebel, Sebastian Pregl, Larysa Baraban, Walter M Weber, Thomas Mikolajick, and Gianaurelio Cuniberti. "Ionic effects on the transport characteristics of nanowire-based FETs in a liquid environment". In: Nano Research 7.3 (2014), pp. 380-389.
- Eunhye Baek, Sebastian Pregl, Mehrdad Shaygan, Lotta Römhildt, Walter M Weber, Thomas Mikolajick, Dmitry A Ryndyk, Larysa Baraban and Gianaurelio Cuniberti. "Optoelectronic Switching of Nanowire-based Hybrid Organic/Oxide/Semiconductor Field-Effect Transistors". Accepted for publication in Nanoresearch

Publications in preparation:

- Julian Schütt, Bergoi Ibarlucea, Sebastian Pregl, Felix Zörgiebel, Walter M. Weber, Thomas Mikolajick, Larysa Baraban and Gianaurelio Cuniberti. "Droplet-based microfluidics meets silicon nanowire sensors". Journal: to be decided
- Lotta Römhildt, Sebastian Pregl, Felix Zörgiebel, Maryam Vahdatzadeh, Yuyu Liu, Bergoi Ibarlucea, Walter M. Weber, Thomas Mikolajick, Jörg Opitz, Larysa Baraban, and Gianaurelio Cuniberti. "Human α-thrombin detection platform using aptamers on a silicon nanowire FET". Submitted to RSC The Analyst or Advances
- Daniil Karnaushenko, Bergoi Ibarlucea, Sanghun Lee, Gungun Lin, Larysa Baraban, Sebastian Pregl, Michael Melzer, Denys Makarov, Oliver G. Schmidt, and Gianaurelio Cuniberti. "Flexible high performance diagnostic platform". Journal: to be decided

Selected international conferences:

- S Pregl, F Zörgiebel, L Baraban, C Richter, and WM Weber, T Mikolajick and G Cuniberti. "Channel length dependent sensor response of Schottky-barrier FET pH sensors". In: Sensors, 2013 IEEE. IEEE. 2013, pp. 1-4.
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Ich versichere hiermit, dass ich die vorliegende Dissertation ohne unzulässige Hilfe Dritter in eigenständiger Arbeit angefertigt habe. Direkt und indirekt übernommene Gedanken und Behauptungen sind gekennzeichnet und mit Quellen belegt. Bei der Durchführung der Arbeit, Herstellung von Transistoren und diesem Schriftstücks habe ich Unterstützung erhalten von den folgenden Personen:

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Sebastian Pregl

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